Power Devices Health Condition Monitoring: A Review of Recent Papers

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ABSTRACT

Power semiconductor devices with adjacent interconnection structures are recognized as the most fragile components of power electronic systems. Condition monitoring addresses this fragility by developing methods and technologies for assessing the component's state of the health. This paper aims to provide entry points to comprehensive, state of the art references on this complex subject, which has been the subject of an extensive research over the last two decades.

An overview of the current state of the art in condition monitoring of power devices (IGBT, MOSFETs) is given with focus on current induced degradation (active thermal cycling). Degradation indicators and temperature sensitive parameters are discussed, as well as their sensibilities to different parameters. Important practical aspects for the use of these indicators in monitoring system are pointed out. The conclusion provides discussion on industrial application perspective of the presented methods.

Index Terms— condition monitoring, failure mechanism, power device, reliability, online health condition monitoring of IGBT / MOSFET, aging, degradation monitoring, wire bond

1. INTRODUCTION

Power converters make use of electronic switches such as IGBTs (Insulated Gate Bipolar Transistor) or MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) to perform efficient energy conversion. However, these power devices are often used in very demanding environments or in modes of operation which challenge their reliability, and therefore are amongst the major components that fail in power converters (Falck, Felgemacher, Rojko, Liserre & Zacharias, 2018; Sathik, Prasanth, Sasongko & Pou, 2019). The lift-off or aging fracture of bonding wire is one of the main reasons for failure of switches in power electronics converters (Hu K., Liu, Yang, Iannuzzo & Blaabjerg, 2020; Yang, Xiang, Bryant, Mawby, Ran & Tavner, 2010). This reliability issue is a threat for the availability of power converters.

Traditionally to improve availability of a power electronic system a regular interval-based maintenance is performed. This can be a good approach to prevent many failures, but it is also expensive as the whole lifetime of devices is not fully utilized. Cost efficiency and high availability are both giving impetus for introduction of health condition monitoring of components to allow CBM (condition-based maintenance) by detecting degradation of components. CBM allows to improve availability while reducing maintenance by considering the actual state of devices which is impacted by operating condition, manufacturing variations, etc.

The approaches of state of health assessment / health monitoring methods of a power device can be broadly classified in the two main categories:

- The condition-based methods based on a failure precursor
- The damage-accumulation-based methods that count and weight the temperature cycles

A third category could be constituted by model-based condition monitoring methods. They operate by comparing output data obtained from the monitored component or system (electrical parameters, response of system, etc.) with those predicted by the model. The result of that comparison can be used to detect degradation of the monitored device. The model can be a digital "twin" of the healthy component or system.

Methods from the first category operate by detecting that some electrical parameter indicative of degradation of the power device has evolved above some limit generally with respect to an initial healthy state. The parameters are typically determined during operation, by online measurements of DSEP (Damage-Sensitive Electrical Parameters), e.g. Vce_on, and TSEP (Thermo-Sensitive Electrical Parameter), e.g. the gate voltage threshold to obtain the junction

temperature Tj. A further processing can be needed to decouple influence of other parameters.

Methods from the second category operate by determining the stress levels, the operating time spent at a given stress level and then use a lifetime model to determine the lifetime consumed by a device. These methods typically perform stress counting based on Rainflow algorithm and determine an "health index" (or SoH: state of health).
The prognostic is a possible next step: it estimates the remaining useful lifetime by extrapolating the current state of health to the future by considering historical usage and expected future usage.

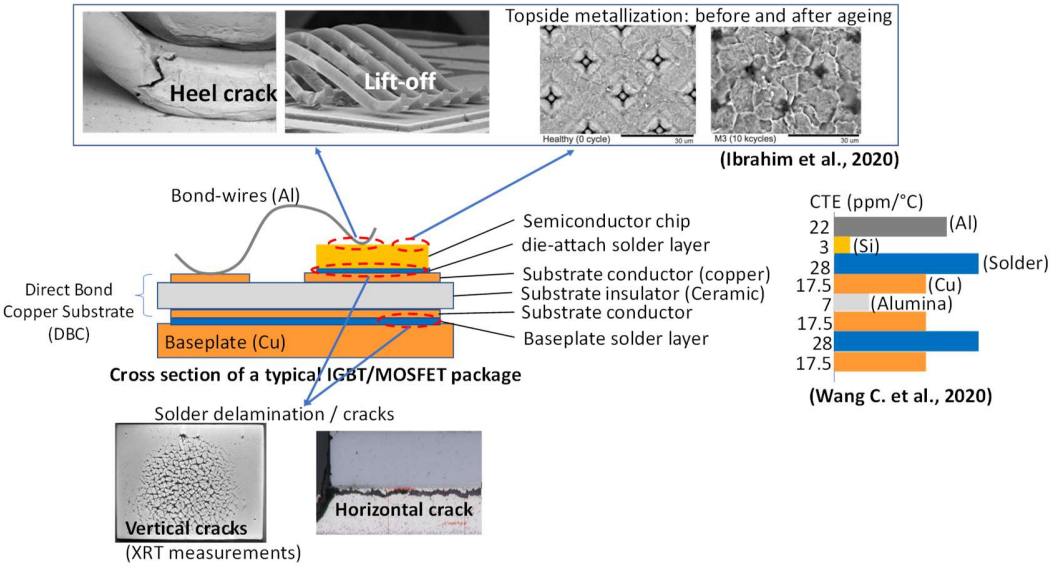

Figure 1. internal structure of wire-bond package IGBT modules and main failure mechanism

The main challenge is how to determine the failure probability of the device as its health index reduces. Prognostic is not further investigated in this review.

The goal of this review is to identify the condition-based methods aimed at detecting incipient wear-out or ageing signs of semiconductors. The detection of catastrophic failures, such as open-circuit or short circuit (Ciappa, 2002) is not in the scope of this review, which can be the ultimate result of the evolution of degradation. A catastrophic failure consequence is that the semiconductor function is completely lost and consequently usually also the full function of the converter (Wu, Blaabjerg, Wang, Liserre & Iannuzzo, 2013).

This paper is organized as follows. First the ageing of power semiconductor devices is shortly presented along with the failure mechanisms and the corresponding degradation indicators. In a second part, different condition monitoring methods are reviewed, classified mostly depending on what type of degradation is monitored. The next section presents practical implementations aspects, and also some online temperature measurement methods. In the last section, the major results are summarized to provide some perspectives from an industrial point of view.

2. AGEING OF POWER DEVICES

2.1. IGBT failure mechanism

Different stressors are responsible of ageing of semiconductor devices. Amongst them the major stressors are temperature related and can be quantified by the junction temperature swing ΔT and the average junction temperature $T_{j,m}$. The voltage stress is also an important cause of failure: transient over-voltage, or over-current, can possibly lead to destruction of device (catastrophic failure) or strongly degrade their lifetime. Also, other factors have an influence on reliability of devices such as humidity, presence of contaminants, vibrations, etc.

The majority of the failure mechanisms encountered in power modules using semiconductor devices (IGBT, diodes or MOSFETS) are related to adjustment of interconnection structures and are driven by thermo-mechanical stresses (Ciappa, 2002). Figure 1 illustrates some degradations caused by thermal cycles, adapted from (Choi, Blaabjerg & Jørgensen, 2018; Ibrahim, Khatir, Ousten, Lallemand, Degrenne & Ingrossi, 2020; Wang, C., Li & Wu, 2020).
Depending on the amplitude of stress (ΔT) and dynamics (duty cycles) of power cycling different failure mechanisms are triggered independently (Baker, Liserre, Dupont &

Avenas, 2014; Smet, Forest, Huselstein, Richardeau, Khatir, Lefebvre & Berkani 2011).

The progressive degradation of IGBTs are mainly of four types:

a) Bond wire fatigue, Degradation of wire bonds (heel cracks, lift-off)
b) Degradation of topside metallizations
c) Degradation of solder die-attach (solder layer fatigue cracks, creation of voids, delamination) between silicon chip & DBC (Direct Bonded Copper)
d) Degradation of gate oxide

The bond wire fatigue is very common in current power modules, as shown in the study of Gutierrez., Lin, DeVoto, and McCluskey, (2019). The degradation of the chip metallization (reconstruction of the aluminum) can also be observed visually after power cycling, and results in an increase in the resistance of the latter. The effect is therefore cumulative with the increase in the resistance of the bond wires at the early stage of their deterioration. According to (Chen, Meng, Zhu, Li & He, 2020) the chip metallization might induce and accelerate the bonding wire lift-off and die-attach solder degradation.
The degradation of solder interfaces can also be observed and leads to an increase of thermal impedance between junction and heath-sink (Z_{THja}). Either the degradation of thermal path, or of the bond wires lead to an increase of junction temperature of semiconductor device (for a given switched current). Finally, the degradation of the gate oxide (Dusmez, Ali, Heydarzadeh, Kamath, Duran & Akin, 2017; Ye, Chen, Wang, Zhai & Vachtsevanos, 2017) leads to a few modifications of the behavior of the power device: increase of gate leakage current, increase of oxide capacitance Cox and a change of threshold voltage $V_{GE(th)}$. It also influences the duration of Miller plateau t_{GP}.

The degradation of semiconductors, by active and passive power cycling, has been experimentally investigated over the past decades and reported in numerous publications such as for instance (Patil, Celaya, Das, Goebel & Pecht, 2009; Ciappa, 2002; Smet et al., 2011; Ibrahim et al., 2020) to name just a few of them. A survey on power cycle testing of power switches is proposed by GopiReddy, Tolbert and Ozpineci, (2015). These power cycling tests have evolved over time to be more and more realistic with respect to "normal" ageing conditions and thus with application-dependent mission profiles reproduce or trigger the same failure mechanisms that are observed in the field on failed components.
In (Patil et al., 2009) a few precursor parameters were identified, following very accelerated thermal overstress tests, such as the increase of threshold voltage with ageing (indicator of gate oxide degradation). The 'on' voltage $V_{CE(on)}$ was shown to reduce with ageing that was found to be correlated to die attach degradation, causing an increase of the p-n junction temperature due to degraded heat dissipation path. The effect of different power cycling protocols on degradation of power modules were studied in (Smet et al., 2011) and it was concluded that ageing mechanisms mainly concern wire bonds and emitter metallization, with gradual impact depending on protocol severity. In (Pedersen, Kristensen, Popok & Pedersen, 2015) the authors were able to correlate degradation of electrical parameters to the development of damage on the microscopic level at wire bonding interfaces.
Ageing monitoring in IGBT module under sinusoidal loading (considered to be realistic ageing conditions) is studied in (Ghimire, Pedersen, Rannestad & Munk-Nielsen, 2015). A rise of on-state resistance, which originates from thermo-mechanical degradation of interconnects on both diode and IGBT, was observed. This in turns creates a positive feedback acceleration of degradation since the increase of power dissipation (due to increase of on-state voltage drop) creates more thermo-mechanical loading in connection, therefore reinforcing the stress. A clear tendency of wire lift-off through partial wire fracturing and wire delamination was observed.

Failure mode depending on technology and applications
The failures observed and the reliability of power modules clearly depend on the type of module considered. In (Wang B., Cai, Du & Zhou, 2017) it is recalled that press pack high-power devices have a higher reliability than wire-bond devices. Evolution of the technology of modules alleviates or can change the major failure modes (for instance using sintering instead of solder between DBC and copper plate, or using spring contacts instead of wire bonds, etc.). Also depending on the application, the failure mode triggered will differ. Failure mode in an inverter is not expected to be the same than for module operating under pulse high-current power cycling application for instance. The peak power processed by power devices in an inverter is generally far less than in a pulse application, but these devices encounter much more thermal cycles during a given operating time. Detachment of the Si/Sn-Ag-Cu (SAC) interface is reported as the major failure mode under pulse high-current power cycling in (Huang, Luo, Xiao & Liu, 2019).
The most studied connection mode, and its degradation due to fatigue, is the wire bonding method.

2.2. Degradation indicators

The degradation indicators, also called partial ageing precursor signals, are derived from analysis of observable electrical signals at the terminal of power modules or delivered by additional sensors (case temperature for instance). Typically, the possible IGBT signals that can be exploited are the gate current (Ig), the collector current (Ic), the collector-emitter voltage (Vce) and the gate-emitter voltage (Vge). In addition, if a kelvin emitter is available, it is also possible to measure the voltage between gate and

kelvin emitter, or between kelvin emitter and (power) emitter (Sundaramoorthy, Bianda, Bloch & Zurfluh, 2014).
The analysis or the control of these signals allows to determine several ageing indicators, described in the abundant literature on the subject. Most of these ageing indicators are listed in Table 1 along with a few relevant references.
The indicators are classified in three categories:

a) Indicators measured outside switching transient (considered "steady state" parameters)
b) Indicators measured during switching ("transient" parameters), i.e. during turn-on or turn-off
c) Temperature based indicators

Table 1. Ageing indicators

a) "steady state"	
Parameter	**references**
Short circuit current Isc (for IGBT only)	(Sun, Gong, Du, Peng, Wang & Zhou, 2017)
Saturation voltage drop Vce_sat	(Avenas, Dupont, Baker, Zara & Barruel, 2015), (Singh, Anurag & Anand, 2017), (Schubert & De Doncker, 2020)
Transconductance g_m	(Wang C., He, Wang, Li & Wu, 2020), (Wang K., Zhou, Sun & Du, 2020)
On-resistance $R_{CE(on)}$	(Eleffendi, & Johnson, 2017)
b) "transient"	
Parameter	**references**
dynamic change of gate current	(Zhou, Zhou & Sun, 2013)
peak gate current value I_{Gpeak}	(Zhou et al., 2013), (Mandeya, Chen, Pickert, Naayagi & Ji, 2019)
Voltage change rate dVce/dt	(Sathik, Prasanth, Sasongko & Pou, 2018), (Kexin, Mingxing, Linlin & Jian, 2014)
Gate-emitter voltage change ΔVge	(Hu Z., Ge, Xie, Zhang, Yao, Dai & Yang, 2019)
Miller plateau duration	(Hu Z. et al., 2019)
Gate emitter threshold or pre-threshold voltage $V_{GE(th)}$	(Mandeya, Chen, Pickert & Naayagi, 2018), (Mandeya et al., 2019)
Current rate of change dIc/dt	(Sathik, Prasanth, Sasongko & Pou, 2019)
c) Temperature based	
Parameter	**references**
Case temperature	(Wang, Tian, Qiao, & Qu, 2016)
junction temperature variation	(Tian, Qiao, Wang, Gachovska, & Hudgins, 2014)
estimation of thermal resistance between junction and ambient R_{thja}	(Hu Z., Du & Wei, 2017), (Zhang J. et al., 2019a)

These degradation sensitive and temperature sensitive parameters differ in sensitivity and in their sensitivity to other parameters' changes. They are discussed in more details in the remaining of the paper.

In (Mandeya et al., 2019), four different DSEPs, respectively Vce(on), Rce(on), $I_{G(peak)}$ and dV_{CE}/dt, are compared in term of their relative sensibility to the virtual junction temperature (T_{vj}) and failure type. The table is reproduced below.

Table 2. Examples of bond wire and chip failure detection techniques

DSEP	**IGBT type**	**Relative sensitivity**		**Immunity to T_{vj} A/B**
		Bond wire / chip failure (**A**)	T_{vj} (**B**)	
$V_{ce(on)}$ [1]	1-chip	1% (bond wire)	0.01%	100 (weak)
$V_{ce(on)}$ [2]	1-chip	14.6% (bond wire)	0.01%	1460 (strong)
$R_{CE(on)}$	2-chip	1.9% (bond wire)	0.44%	4 (weak)
$I_{G(peak)}$	2-chip	36% (chip)	0.05%	720 (medium)
dV_{CE}/dt	2-chip	25% (bond wire)	0.17%	147 (weak)

[1]: $V_{CE(on)}$ is the on-state voltage drop under load current
[2]: $V_{CE(on)}$ is the on-state voltage drop at the inflexion point

$$Relative\ Sensitivity = \frac{|Variation|}{Baseline\ value_{room\ temperature}} x100\% \quad (1)$$

The relative sensitivity is calculated as shown in Eq. (1). Table 2 shows that the on-resistance $R_{CE(on)}$ is clearly the most impacted by T_{vj} variation, that is to say it has a rather high temperature dependence. Its "immunity" to T_{vj} is considered weak because of the low ratio (A/B), i.e. the relative sensitivity of $R_{CE(on)}$ to degradation is not so high compared to its relative sensitivity to temperature. This parameter cannot therefore be used as a DSEP without precisely compensating for its sensitivity to T_{vj}. From that point of view, Vce(on), the on-state voltage drop under load current, and the rate of change of Vce (i.e. dVce/dt) are still not so immune to junction temperature. Other indicators show better immunity to T_{vj} such as $V_{CE(on)}$ measured at inflexion point (not sensitive to temperature theoretically) and $I_{G(peak)}$, to a lesser extent, and present a good sensitivity to bond wire degradation, therefore they constitute interesting DSEPs (Mandeya et al., 2019).

Apart from indicators seen above, a few less covered techniques are also present in the state of the art, for instance based on modification of the transient characteristics ringing of output signals as in (Ginard et al., 2009).

3. CONDITION MONITORING METHODS

The purpose of on-line health condition monitoring of IGBT is to extract health status during regular operation of the

converter, and then determine the health level of the devices. Only the ageing degradation is of interest here: sudden failure (e.g. device short-circuit) more belongs to the scope of protection and is not covered here.
As shown in section 2.2, several IGBT's electrical parameters are affected by ageing and these indicators can be used by different methods to determine health state of a device. A classification of indicators for different degradations of IGBT modules is proposed in review (Hu K. et al., 2020).
The methods are classified in term of degradation failure mode: bond wire, solder, metallization and gate oxide. For each failure mode a few failure indicators are considered. This can be summarized in Table 3.

Table 3. Indicators for different degradations in IGBT modules (adapted from (Hu K. et al., 2020)).

Degradation failure type	**Indicator**	**Description**
Bond wire	Vce_on	Vce on state voltage
	$Vce_{turn-on}$	Vce during turn-on
	VeE	Voltage between kelvin and power emitter
	t_{GP}	Miller plateau duration
Solder	R_{THjc}	Thermal impedance (junction to case)
	T_j	Junction temperature
	5th harmonic	analysis of impact on output voltage
	dVce/dt	Rate of change of Vce
	dIc/dt	Rate of change of Ic during turn-on or turn-off
Metallization	Vce_on	On state voltage
Gate oxide	Vth, $V_{GE(th)}$	Gate threshold voltage
	t_{GP}	Miller plateau duration

The ageing of the device results in the change of its terminal electrical characteristics (increase of resistance of bond wires, also change of inductance in case of wire bond lift-off, etc.).

The different considered ageing indicators are generally also impacted by other variables or even different degradation modes (Avenas et al., 2015) that must be considered. For instance, the on-state voltage measured across power device terminals is impacted by collector current (Ic) and junction temperature (Tj).

A separation strategy with respect to these parameters is proposed in (Kong, Du, Ouyang, Wei & Hurley, 2019) where measurement of on-state voltage is decomposed into a dependent (to failure) part and two independent parts, function of temperature and current. The independent parts in the failure prediction can be removed, making it possible to obtain the voltage variations caused by bond wire failure.

However, the need for such extensive off-line pre-calibration makes this method difficult to apply in practice.
Further, different kind of failures might affect the same indicator (and not necessarily with the same trend). An example of indicator that has opposite variation trend is t_{GP} (duration of Miller Plateau): its duration is increased in case of gate oxide degradation due to increase of Cox, and is reduced in case of wire bond lift-off, due to reduction of gate-emitter capacitance.

3.1. Wire bonds degradation detection

Bond wire degradation starts with an increase of resistance and ultimately ends as lift-off.
Wire bonds lift-off tends to increase the resistance (ΔR) seen between collector and emitter during on-state. A very common method to detect this kind of degradation is based on monitoring of V_{CE_on} which tends to increase when considered at a given temperature and switched current: $V_{CE\_on}=f(Tj, Ion, \Delta R)$.
It is desirable to operate at large current for this method, while current also influences in that case Tj due to self-heating of device. It is important that current be constant during measurement which is difficult to achieve in application.

A wire bond degradation detection method based on On-resistance $R_{CE(on)}$ can be found in (Eleffendi & Johnson, 2017). The main drawback of this method is that it is sensitive to temperature variation, which is difficult to compensate. The method is not very sensitive to early degradation signs since it was not able to detect first bond-wire lift-off.
Remark that the degradation of metallization may also slightly contribute to the increase of V_{ce_on}, or measured $R_{CE(on)}$. Since it would affect the parameters with the same trend this is not a problem for the purpose of degradation detection (if not interested by the exact source of degradation).

The availability of a kelvin emitter (respectively kelvin source for MOSFET) enables a more accurate detection of wire bond degradation, since it is possible to exclude influence of forward voltage which might also be impacted by ageing, but not necessarily with the same trend (Baker, Luo & Iannuzzo, 2017). Note that voltage between kelvin emitter and emitter (VeE) normally has low amplitude, due to the very low resistivity of wire bonds, and is affected during transient by the inductive nature of this type of connection. This is not an issue for measurement in "steady state", i.e. past the switching transient. Note that the inductive nature of the parasitics between kelvin emitter and emitter (stray inductance and small series resistance) is sometimes exploited to perform current measurement or detection during transients (similar to a measurement with a Rogowski coil, by detecting di/dt). The increase of stray inductance between source and auxiliary source is used to detect bond wire lift-off in (Gonzalez-Hernando, San-Sebastian, Garcia-

Bediaga, Arias, Iannuzzo & Blaabjerg, 2018). The same authors then proposed a method still based on the measurement of the voltage drop V_{SauxS} (MOSFET) but considering only the increase in the resistivity of the bond wires caused by their degradation (Gonzalez-Hernando et al., 2019).
Other methods, which are not indicated in Table 3, are reported in the literature. For instance, a method based on short circuit current (Sun et al., 2017a) can detect degradation of device considering that the peak amplitude of short circuit current tends to reduce with ageing.

Transconductance (g_m) variation as ageing indication is demonstrated in (Wang C. et al., 2020), (Wang K. et al., 2020). The method requires however a temperature compensation since transconductance g_m (in A/V) decreases as temperature rises; this decrease has however been shown to be quite linear with temperature. As the bond wire degrades (increasing number of bond wire lift-off) g_m slightly drops and Ic also drops for a given Vge. At given measurement Ic current, Vge is increased with ageing.

After temperature compensation g_m is only impacted by the number of wire bond lift-off (reduction with respect to initial gm ≈ -0.7% by wire bond lift-off).

Miller plateau duration can also be used as indication of degradation of wire bonds: its duration is reduced with ageing (Hu K. et al., 2020). An explanation of the influence of ageing of IGBT wires bond wires on Miller plateau voltage and its duration can be found for instance in (Kong et al., 2019).

3.2. For detection of solder fatigue (degradation of solder interfaces)

The degradation of solder die attach leads to a degradation of the thermal path between die and heat sink which increases equivalent internal thermal resistance Rth and thus of junction temperature Tj. It also impacts some electrical parameters of the device. A degradation of the DBC solder leads to the same results. An increase of R_{thja} might be due also to a degradation of TIM (thermal interface material) interface between module and heatsink: the determination of exact cause of degradation is not necessarily easy. However, any degradation of thermal path tends to increase the die temperature for a given processed power and thus acts as positive feedback for further degradation.
Note that both major degradation modes (bond wire lift-off and solder fatigue) lead to an increase of Tj: either due to increase of losses (increases resistance of wire bonds/metallization; increase of current density in remaining wire bonds) / degradation of Rth (solder fatigue) and thus increase of temperature for a given power loss in power device).

The increase of rate of change (dIc/dt) has also been proposed in (Sathik et al., 2019) as an indicator of solder fatigue.
In (Tian et al., 2014) the instantaneous junction temperature of an IGBT is estimated from a thermal network model. The "healthy" thermal model is initialized by an initial calibration procedure while the device is still in healthy state. The health condition is estimated by the variation between present temperature and the calculated initial temperature using the "heathy" thermal model, when operation is performed at same current. The method requires to measure Vce, Ic anc Tc (case temperature). Vce and Ic are used to calculate the losses Ploss used to feed the thermal model.

In (Zhang J. et al., 2019a), (Du, Li, Zhang, Tai, Sun & Zhou, 2016), (Zhang J. et al., 2019b) the authors present a quasi-online method to identify the thermal network parameter based on study of cooling curve of junction temperature of power module (during converter shut-down). These methods use Vce on as TSEP (Tj is recomputed from the pre-established voltage–temperature relationship); Heat up is created by normal operation of the converter or special operation to create desired temperature increase due to losses in semiconductors. Cool down is of course affected by cooling system and the temperature of the heat-sink has also to be monitored during that phase. The presence of a controlled temperature cooling system, in a power cycling test bench typically, helps to reduce the cooling time down to coolant temperature. This make the measurement easier and avoids a too long shut down of equipment that may not be convenient in the field.

In (Du et al., 2016) the parameters of Cauer network are extracted by solving analytical equations derived considering the electrical-thermal analogy. Two different cooling curves, measured at two different cooling conditions, are required to solve the equations. This would be the most restrictive point for any system (different from a temperature-controlled ageing test bench), since to obtain different cooling conditions it is required to change fan speed or water velocity for instance.
In (Zhang J. et al., 2019b) the authors have shown experimental results using the method to identifier the Cauer model parameters to validate the feasibility and accuracy of this approach.

The case temperature has been used in (Wang et al., 2016) to detect the increasing non uniformity in the case temperature due to degradation of solder. Two temperature sensors were used: one below the chip (Tc_{chip}) and one near the chip (Tc_{side}). With the number of thermal cycles Tc_{side} tends to decrease while Tc_{chip} increases (also Tj). This is correlated to the degradation of thermal interface between the die and the case (increase of R_{thjc}).

3.3. Combined diagnosis of wire-bond lift-off and solder fatigue

This is the case for the method proposed in (Eleffendi & Johnson, 2017). This paper presents an approach for estimating the extent of solder fatigue and wire-bond lift-off degradation in power semiconductor packages based on online monitoring of the thermal resistance R_{thja} and the electrical resistance R_{CE} (the dynamic resistance of the forward characteristic of an IGBT). In order to estimate these two parameters, two techniques are used: a residual obtained from a Kalman filter, which estimates the change in the thermal resistance R_{thja}, and a recursive least squares algorithm, which is used to estimate the electrical resistance. Z_{thja} (and consequently R_{thja}) is determined by monitoring the cooling phase of the IGBT monitored (heat sink maintained at a constant temperature). Vce measured at low current is used as TSEP during the monitoring.

Also in (Singh, Anurag & Anand, S. 2017), (González et al., 2019) the authors address the degradation assessment of power module by online monitoring of two damage indicators: the on-state voltage V_{DSaux} of the semiconductor (MOSFETs) and the voltage drop in the bond wires, V_{SauxS} measured between auxiliary source Saux and source S. The on-state voltage of a semiconductor can be employed for temperature estimation, in order to anticipate failures in the solder joints that increase the thermal resistance of the cooling path. Moreover, by measuring the voltage drop in the bond wires, the degradation of the bond wires can be detected. The technique employed requires special operating regime (keep MOSFET in on-state for a duration ≈ 200 µs to allow measurement) which can be considered as a minor disturbance of regular operation due to the short duration.

3.4. Choice of ageing indicators

Different DSEPs have different level of sensitivity to ageing and can thus provide quite variable identification accuracy. It is obviously desirable to select a DSEP with a high sensitivity to the expected degradation mode monitored. For IGBT monitoring the increase in the on-state voltage drop (Vce_on) and the thermal resistance (R_{thja}) are the most significant changes in the terminal characteristic (Degrenne, Ewanchuk, David, Boldyrjew & Mollov, 2015).
This is not the only aspect to consider. A tradeoff between several constraints and objectives, generally contradictory, must be done when choosing method for industrial application: cost, complexity, precision, etc. Many practical problems must be solved considering the constraints of a power converter: measurement of small signals (tens of millivolts…) / signal fluctuations due to noisy environment (interferences); need for high resolution, high sampling rate ADC if implemented in digital. Consequently, some methods are not applicable, or really borderline, for on-line monitoring.

Moreover, most of the ageing indicators are sensitive to several variables that must be measured accurately too since their inaccuracy will affect the accuracy of the indicator. The load conditions can also affect some parameters, such as the switching transients for instance.
It is also noticeable that most degradation indicators are TSEPs (temperature sensitive electrical parameters) as well. Temperature must be generally known to enable degradation assessment. It is therefore important to be able to determine this temperature independently of the ageing state of the device. This can be achieved either by considering parameters independent of ageing (using the internal gate resistance as TSEP for instance), or by decoupling ageing from temperature effect in considered ageing indicator.

Considering the commonly used Vce_on parameter, this one can be used as TSEP when measurement is done at low collector current (Ic) since the voltage Vce_on is not significantly influenced by ageing state of the device in that case (very low voltage drop in ΔR).
It is also sometimes possible to compensate the impact of ageing as performed in (Degrenne & Mollov, 2019) where the increase of Ron (due to successive wire-bond lift-off) is estimated so as to correct the value of Vce_on when used as TSEP. The correction was permitted by a special routine using existent hardware: the voltage drop at a reference coolant temperature and current was used to estimate the electrical resistance increase.

To measure a DSEP independently of temperature one possibility is to consider measurement at a particular point not affected by temperature (point ZTC, for zero-temperature-coefficient) (Peng, Sun, Zhou, Du & Cai, 2017; Degrenne & Mollov, 2018; Degrenne, Kawahara & Mollov 2019; Singh et al., 2017). This approach is critically reviewed in some publications as for instance in (Kong et al., 2019) where the authors consider that it is a big challenge to apply Vce-int (Vce value at intersection point between curve measured at different temperatures during pre-calibration) to predict IGBT module bond wire in other working conditions. This approach has however been successfully applied for instance in (Degrenne & Mollov, 2018; Degrenne et al., 2019). In addition, the authors explain the self-calibration procedure employed to determine the ZTC point which is device specific.

The ZTC point is the intersection point on the graph (Fig. 2).

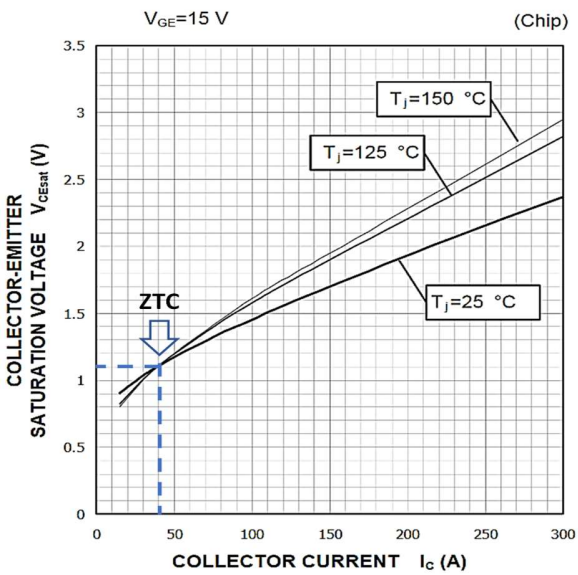

Figure 2: typical static characteristic of an IGBT (from CM150TX-24S datasheet)

It is shown (Peng et al., 2017) that the collector current reduces with the degradation of bond wires and remains constant under different junction temperature. In (Degrenne & Mollov, 2018) this measurement method was used in a power cycling test bench to detect on-line the lift-off of wire-bonds. It was shown that detecting a single wire bond lift-off is challenging.

The failure criteria corresponding to 5% increase of Von at high current could be easily detected (35 mV increase at ZTC current) in (Degrenne et al., 2019).

In (Singh et al., 2017) the same method is used for diagnosis of discrete packages IGBTs (not within power modules). The wire bond degradation condition monitoring method operates as follows. First the inductor current I_L and $V_{CE,on}$ of each IGBT are sensed. Then if (I_L==$I_{inflexion}$) and ($V_{ce,on}$>$V_{ce,critical}$) then the IGBT is considered failed, otherwise the procedure is restarted.

In the following section different practical aspects for the measurement of various indicators are discussed.

4. PRACTICAL IMPLEMENTATION OF MONITORING DEVICES

A comparison in term of advantages and shortcomings of the different damage indicators can be found in (Avenas et al., 2015). This qualitative comparison considers for instance criteria such as the maturity of indicator (i.e. investigated more or less in depth in scientific literature), the conditions for applicability (off-line, online) and constraints or requirements.

A recent paper (Nguyen & Kwak, 2020) also makes a fairly detailed review on the implementation of different indicators (either DSEPs or TSEPs), considering the hardware for sensing circuits. We thus do not develop this exhaustively here, but rather highlight the important points on the techniques presented. Off-line solutions are excluded from the study.

4.1. Gate side monitoring

For these methods the signal conditioning is less challenging due to the limited voltage range. However, the acquisition still presents different potentials problems: noise, presence of significant common mode voltage for the upper switch, possibly also the need for high resolution ADC. This last point can be eventually alleviated by using some analog conditioning circuits to select part of interest in signal, as in (Van Der Broeck, Gospodinov & De Doncker, 2018) for instance, but this comes with added hardware.

4.1.1. duration of Miller plateau

In (Liu, Zhang, Chen, Qi, Qin, Wang & Geng, 2018) the duration of Miller plateau during turn off is rather used as an ageing indicator. It is shown that as the bond-wire degradation develops and the junction temperature rises in the aging process, the Miller plateau width decreases. This parameter is both temperature and degradation sensitive. It is also significantly affected by collector current which has to be known. The hardware needed to trigger the start and end of measurement is quite simple (comparisons of gate voltage level). However, since the variation of duration due to ageing is relatively limited, a high resolution time measurement is required: even by slowing down the turn-off time by using a large external gate resistance Rg=100 Ω, a sensitivity of about 1.8 ns/°C was obtained (only 0.13 ns/°C with Rg=10 Ω). The authors have used a dedicated integrated circuit to perform time to digital conversion with 90 ps of typical resolution. The temperature sensitivity is rather low but increases with the value of the gate resistance.

This method is considered applicable to all types of MOS-gated devices including SiC power MOSFETs. The limit value considered for end of life criterion requires further research.

In (Liu, Zhang, Chen, Qi, Geng & Wang, 2019) the plateau time duration during turn on is analyzed. Again, the indicator is used as TSEP rather than DSEP. Theoretical analysis and experiments have demonstrated the adverse effects of package-related bond wire fatigue and chip-related gate oxide degradation on the Miller plateau duration. The paper proposes a hardware circuit to process gate voltage in order to generate the trigger signals used for time measurement, but that circuit is limited to low switching speed applications. Amongst the practical issues, it is underlined the need for an accurate preliminary calibration. Also, the operating point must be considered to avoid masking effect and enable ageing assessment.

4.2. Collector-emitter side monitoring

4.2.1. Vce_on monitoring

This measurement is challenging for many reasons. The useful signal (during on-state) is only a few volts while voltage in blocked state is very high. Further, due the sensitivity of the indicator, a good resolution is needed. For example, in (Degrenne & Mollov, 2018) a SAR ADC with 18-bit resolution was used. In this latter publication a Von measurement circuit is described, including the components references used. The estimated cost is not given but can be easily determined for the part list. The acquisition process is detailed as well as motivation for oversampling. Detection of Von value is performed by considering values delivered by ADC, when they are inferior to three volts.

In (Degrenne et al., 2019) the cost of monitoring for a half-bridge is optimized by using analog switches to multiplex the two measurements and thus use only one ADC & Isolator. The cost for the acquisition hardware is estimated to less the 8 euros. The processing must still be performed in a FPGA or processor, interfaced to the isolator (a command is also required to control the multiplexor).

Other circuits can be used to perform Vce_on monitoring. The choice depends on voltage level considered and desired accuracy and cost tradeoff. A comparison of the different circuit can be found for instance in (Hu K. et al., 2020).

4.2.2. Short circuit-monitoring (Isc)

Short circuit method requires to create a short duration short circuit for instance during 5 µs to assess the ageing state, considering that short circuit current is reduced with degradations. In (Sun et al., 2017b) a method is proposed to perform simultaneously the DC capacitors diagnosis (ESR estimation) and the power devices by creating such short short-circuit. It consists in creating a short duration short-circuit of DC-bus though a leg being tested. The impact of the short circuit on DC bus is almost unnoticeable (very short duration, “limited” short circuit current and large DC bus capacitance) and only affect very moderately the output voltage. The small disturbance of DC bus voltage is however used to estimate ESR (voltage drop ESR*Isc). The long-term reliability of the IGBT might be compromised however if this kind of monitoring is performed too often.

4.2.3. Current measurement on collector side

Current on collector side (Ic) must be monitored in most cases: for short current current measurement (Isc), or simply because it influences the measured indicator, Vce_on for instance, and must be known. For some cases, only the di/dt might be of interest, for estimation of chip solder layer fatigue for instance (Sathik et al., 2019). Different kind of current sensors can be used for that purpose (Hall-effect, shunt, Rogoswki coil based, voltage across package parasitics to measure derivative of current).
Shunt based measurement is simple but adds some losses and a possible cause of unreliability (can possibly fail open and is in series with power devices).
Hall effect sensors are quite expensive (in closed-loop version) and suffer from potential bandwidth limitation.
Methods based on voltage measurement across parasitics (VeE for instance) have the potential limitation that some variance may be observed even on same type of components from a manufacturer over time (change of module generation, internal bond-wires layout…)
On the other hand, Rogowski coil sensors present the advantage of being very low cost, large bandwidth sensor particularly adapted for di/dt measurement. They are also non-intrusive, isolated, non-saturable and can be produced using PCB with very well controlled characteristics. Their main drawback is the need for integration circuit when used for current measurement.
Alternatively, Ic might be calculated considering the switching state of device and output current if this one is known.

4.3. On Tj measurement or estimation

Solutions that require a modification of the semiconductor device, an alteration of the package or which embed a sensor on the chip surface are not covered here (diode, thermistor, thin thermo-sensitive polysilicon layer, etc). The methods of interest must allow to estimate the junction temperature while being the less invasive possible.

Basically, there are two main practical methods to determine (or rather approximate) the junction temperature Tj

1) Using a thermal model fed by the calculates losses in the device
2) using TSEP to determine the junction temperature

The first method requires to be able to calculate accurately the losses within the device which is not necessarily easy, and to first determine a thermal model of the device (considering its cooling environment and ambient temperature). Since the electrical and thermal interface of module evolves with time the calculation is not valid during the whole lifetime of module (Baker et al., 2014).

The second method requires calibration if absolute temperature is to be estimated.
These methods allow to calculate an average temperature across the die, not the peak temperature of the die (hotspot).

4.3.1. TSEP for Tj estimation

Some methods require specific operating conditions or modification of power converter to be applicable, as for instance the on-state voltage drop (Vce_on), measured at low current, to avoid self-heating and influence of ageing.

This condition can be met for instance in an inverter application, when the output current crosses zero.

It is sometimes also required to modify the control, or to slow it down (increase of gate resistance for instance) so that measurements of temperature can be performed.

A list of several on-line TSEP based methods that do not require alteration of converter operation is given in (Degrenne et al., 2015), with the associated sensitivity, recalled below in Table 4.

Table 4. On-line TSEP based methods

Method	**Sensitivity (**approx.)
Voltage at high current of transistor or diodes (based on impact of temperature on static I(V) characteristic) (Tsukuda, Guan, Watanabe, Yamaguchi, Takao & Omura,, 2020)	20mV/K
Turn-off transition time of IGBT transistors (Kuhn & Mertens, 2009).	2 ns/K
Turn-on delay time (td_{On}) (Kuhn & Mertens, 2009)	2 ns/K
di/dt of transistors (Sundaramoorthy et al., 2014)	40 A/(µs.K)
Threshold voltage of MOS transistors (applicable to IGBT)	10mV/K
Peak current measurement: I_{Gpeak} method (Baker, Munk-Nielsen, Iannuzzo & Liserre, 2016)	2.5mA/K

Other TSEP exist such as the variation of dynamic characteristics with the temperature of the device (Baker et al., 2014), or the reverse voltage peak between the auxiliary emitter and power emitter measured upon IGBT turn off (Zhang J. et al., 2019b).

Note that some of these parameters are also sensitive to degradation of device (DSEP): voltage drop of transistor for instance. Short circuit current, for a controlled duration, is also sensitive to Tj (Ceccarelli, Wu, Iannuzzo, 2019) and is impacted by ageing.
The key of a good TSEP is in independence with respect to other factors (ageing in particular).
In his PHD thesis (Mandeya, 2019) related to on chip failures identification in multichip IGBT power modules, the author performs a very detailed analysis and comparison of many TSEPs and proposes a few additional ones. In his context, the Vge voltage at pre-threshold level ($V_{GE(pre-th)}$) appears as a good candidate and was used for his studies. What is called "pre-threshold" voltage is not exactly the same as threshold voltage: it is measured at turn on slightly before $V_{GE(th)}$ is reached. One of the claim advantages is that since current has not started to flow through the device there is no self-heating. The measurement point corresponds to a given delay after the gate turn-on command.
The threshold voltage is sensitive to ageing too (Celaya, Vashchenko, Wysocki, Saha & Goebel 2010).
The reader will find another comprehensive survey of TSEP in (Baker et al., 2014). This paper recalls also several issues for the practical use of TSEP. The first one is the need for calibration (typically performed by imposing temperature to the devices by an external system). It is underlined that even a small error on measurement can lead to a significant error on temperature estimation. Another important issue is created by the connections: there is no direct access to junction voltage drop for instance which leads to temperature estimation error due to wire bonds temperature and impact of ageing. This impact of ageing on some TSEPs might not be a significant issue in laboratory environment where recalibration to maintain accuracy of measurement is always possible but is a more serious issue in a field application. Considering impact of ageing process on considered TSEP appears as a better practical option: for instance, by estimating the increase of wire-bond resistance with ageing to correct Vce_on measurement.

In (Tsukuda et al., 2020) an acquisition system is used to monitor in real time V-I curve for both switching device and diode with case temperature and the data is stored on board memory and can be monitored on-line.

The reverse voltage peak between the auxiliary emitter and power emitter (measured during IGBT turn off) has been shown to be a dynamic TSEP measured during turn-off process (Zhang J. et al., 2019b). The negative rate of change of collector current during turn-off induces a negative voltage pulse on VeE. The amplitude of the (negative) peak, $V_{eE\text{-}peak}$, is shown to be impacted by both temperature and switched current level Ic. Thus, at a given current Ic, the peak amplitude (in absolute value) linearly decreases as temperature rises.
The amplitude of this peak (in absolute value) increases with increasing value of Ic. A better sensibility is obtained at large collector current.

Some TSEPs and associated monitoring techniques are presented in the following sections.

4.3.2. Gate current measurement

The dynamic changes of the gate current with ageing of IGBT have been studied in (Zhou et al., 2013), with simulated ageing by cutting the bond wires.
The peak gate current measurement during turn-on is now quite popular and is classically used as TSEP to estimate junction temperature (Baker et al., 2016, 2017).

A study of its accuracy of this method can be found in (Baker et al., 2017). In this paper, the gate current is measured across

the external gate resistor and requires thus a differential amplifier. Alternatively, for the measurement of this current, a current mirror can be used as in (Baker et al., 2016).
The peak current is then detected using a resettable peak detector.
The main limitation of the technique is that detecting accurately the peak gate current value is difficult in practical applications (small signal, electromagnetic interferences)

Combined with Vge voltage measurement, the gate current can be used to estimate R_{Gint}, the internal gate resistance.
One advantage of this resistance is that it constitutes a good TSEP while being very insensitive to ageing.

4.3.3. Gate voltage plateau sensing

A method based on acquisition of gate voltage plateau sensing during turn-on is presented in (Van der Broeck et al., 2018). Relation between this voltage and temperature has to be established at known device currents (calibration phase).
The sensing circuit proposed is composed of three stages, respectively a differential amplifier to reject common mode voltage of gate voltage, an active rectifier followed by a filter to select the signal part of interest, and finally a resettable integrator stage that operates during desired time window. This method gives a sensitivity between 1.5 and 7 mV/K.

4.3.4. Turn-off delay time

In (Li et al., 2017), (Luo, Chen, Sun, Li & He, 2016), (Zhang Z. et al., 2019) the turn-off delay time (td_{Off}) is considered.
Vge, Vce and Ic must be measured.
In (Li et al., 2017) the duration of td_{off} is measured during turn off starting when Vge reaches 90% of Vge_{max} until Vce reaches 90% of Vce_{max}. Comparators and voltage references are needed to perform detection as well as isolation circuit. Duration of turn-off delay time can then be determined by a digital circuit (FPGA / DSP).
Calibration must be performed at different level of Ic, supposing a fixed Vdc voltage (otherwise it must be considered too). This method can be applied on-line. In (Luo et al., 2016) the parasitic inductor L_{eE} between the Kelvin and power emitter terminals of an IGBT module is utilized to extract the turn-off delay time. The analysis of that voltage alone is enough to determine td_{off}. Some comparators and threshold references must again be used to determine start and end of turn-off phase. Sensitivity is around 4ns/K which implies that duration can be measured with at least that resolution (for 1 °C resolution in temperature measurement).
In (Zhang Z. et al., 2019) the method is used for SiC power devices and the method exhibits a lower sensitivity around 0.7 ns/K despite the use of a gate impedance regulation assist circuit used to strongly enhance the sensitivity. That circuit mainly slows downs the slew rate of gate source voltage. A higher resolution time measurement is also required for this device.

4.3.5. Threshold voltage

The threshold or quasi threshold voltage is determined by considering the gate to auxiliary emitter voltage and the voltage between the auxiliary emitter and the power emitter (Ccoa, Strauß, Mitic & Lindemann, 2014), (Bahun, Čobanov & Jakopović, 2011), (Griffo, Wang, Colombage & Kamel, 2018). The determination of that indicator thus requires measurement on control and power side of the IGBT.

In (Ccoa et al., 2014) different TSEPs of an IGBT have been studied. A method to measure the threshold voltage in on-line mode has been evaluated. The sensitivity, rather low, is around -29.9 uV/K. A good resolution ADC is thus required. The proposed method for the measurement is to sample the gate voltage (between gate and kelvin emitter) when voltage between emitter and kelvin emitter exceed some negative threshold (proportional to dIc/dt upon start of conduction of IGBT) This method can be implemented in the driver board.
In (Bahun et al., 2011) the quasi-threshold voltage using dedicated modified gate driver circuit is used for real time virtual junction temperature estimation. Sensitivity is around -10 mV/K for IGBT. As in (Ccoa et al., 2014) the detection of a voltage across parasitic inductance between kelvin emitter and emitter is used to detect start of conduction. The authors call the corresponding gate voltage level, “quasi-threshold” level since it is not measured in the standard way.
In (Griffo et al., 2018) the same technique is used for SiC power MOSFETs. Other TSEP methods are also evaluated on this type of component.

4.3.6. Measurement based on the on-chip internal gate resistor

In (Denk & Bakran, 2015) the identification is performed during the off-state of IGBT: the temperature is determined by superimposing the negative gate-emitter voltage with a high-frequency identification signal. The AC injection is performed by enabling an AC source in series with blocking DC voltage. The response is determined by processing the gate current, measured by voltage drop across the external gate resistor. The signal conditioning further consists in extracting the rms value of identification signal, suppressing its dc offset and then scaling before sampling by ADC.
In (Denk & Bakran, 2017), a similar method is used to measure the internal gate resistance, but the on-state voltage is also measured as well as the collector current.

In (Brandelero, Ewanchuk & Mollov, 2018) the virtual junction temperature is estimated by injecting a DC current into the gate path of the power die and measuring the voltage across the gate emitter. This also allows to determine the value of the internal gate resistance. The proposed method employs a simple modification to the classical gate driver configuration. Two different schemes are proposed for measurement during either on-state or off-state of the device. The method was shown to have low sensitivity to DC bus

voltage when measurement is performed during on-state and operates on-line without modification of output PWM pattern.

5. CONCLUSIONS

This paper shows that huge research work has already been done in this field of condition health monitoring of power devices. However, there are still many challenges to combine a good detection sensibility, limit the complexity and cost of these methods, to allow more frequent integration into power converters and thus enable CBM.

Perspectives / trend

TSEP and DSEPS are closely linked: most degradations (wire bond / solder fatigue) lead to an increase of device junction temperature Tj. Likewise, most of the electrical parameters impacted by aging are also temperature sensitive. Therefore, one of the challenges for degradation diagnostic is to select a TSEP that is little impacted by aging and a DSEP which has good sensitivity to expected degradation (Bond wires degradation appears to be the most relevant degradation mode to track for actual power modules). Another possibility is to perform degradation monitoring at a particular operating point where the influence of temperature is negligible (zero temperature coefficient, ZTC.

The choice amongst the different indicators is not trivial because of the sensibilities of some of them to other parameters (switched current, blocking voltage…). A "good" choice should allow to minimize influence of these factors which is made challenging by the will to limit the complexity and cost (number of required sensors and associated conditioning) of the monitoring system.

From an industrial perspective point of view, the adoption of condition monitoring for power devices would be facilitated, in term of cost and ease of use, if such functionality would be embedded in "intelligent gate driver". From that point of view, methods that can derive TSEP/DSEP from the gate side (voltage / current) are clearly good candidates.

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REFERENCES

Avenas, Y., Dupont, L., Baker, N., Zara, H., & Barruel, F. (2015). Condition Monitoring: A Decade of Proposed Techniques. IEEE Industrial Electronics Magazine, 9(4), 22–36. doi: 10.1109/MIE.2015.2481564

Baker, N., Luo, H., & Iannuzzo, F. (2017). Simultaneous on-state voltage and bond-wire resistance monitoring of silicon carbide MOSFETs. Energies, 10(3), 1–8. doi: 10.3390/en10030384

Bahun, I., Čobanov, N., & Jakopović, Ž. (2011). Real-time measurement of IGBT's operating temperature. Automatika. doi: 10.1080/00051144.2011.11828429

Baker, N., Liserre, M., Dupont, L., & Avenas, Y. (2014). Improved reliability of power modules: A review of online junction temperature measurement methods. IEEE Industrial Electronics Magazine, 8(3), 17–27. doi: 10.1109/MIE.2014.2312427

Baker, N., Munk-Nielsen, S., Iannuzzo, F., & Liserre, M. (2016). IGBT Junction Temperature Measurement via Peak Gate Current. IEEE Transactions on Power Electronics, 31(5), 3784–3793. doi: 10.1109/TPEL.2015.2464714

Baker, N., Dupont, L., Munk-Nielsen, S., Iannuzzo, F., & Liserre, M. (2017). IR camera validation of IGBT junction temperature measurement via peak gate current. IEEE Transactions on Power Electronics, 32(4), 3099–3111. doi: 10.1109/TPEL.2016.2573761

Brandelero, J., Ewanchuk, J., & Mollov, S. (2018). On-line virtual junction temperature measurement via DC gate current injection. CIPS 2018 - 10th International Conference on Integrated Power Electronics Systems, 423–429.

Ccoa, J. A. B., Strauß, B., Mitic, G., & Lindemann, A. (2014). Investigation of temperature sensitive electrical parameters for power semiconductors (IGBT) in real-time applications. PCIM Europe Conference Proceedings, 2014-May, 456–464.

Ceccarelli, L., Wu, R., & Iannuzzo, F. (2019). Evaluating IGBT temperature evolution during short circuit operations using a TSEP-based method. Microelectronics Reliability, 100–101(July). doi: 10.1016/j.microrel.2019.113423

Celaya, J. R., Vashchenko, V., Wysocki, P., Saha, S., & Goebel, K. (2010). Accelerated aging system for prognostics of power semiconductor devices. AUTOTESTCON (Proceedings), (October), 118–123. doi: 10.1109/AUTEST.2010.5613564

Chen, Y., Meng, F., Zhu, A., Li, W., & He, X. (2020). Chip Metallization Aging Monitoring with Induced Voltage veE between Kelvin and Power Emitter for High Power IGBT Modules. ECCE 2020 - IEEE Energy Conversion Congress and Exposition, (51925702), 4012–4016. doi: 10.1109/ECCE44975.2020.9236104

Ciappa, M. (2002). Selected failure mechanisms of modern power modules. Microelectronics Reliability, 42(4–5), 653–667. doi: 10.1016/S0026-2714(02)00042-2

Choi, U. M., Blaabjerg, F., & Jørgensen, S. (2018). Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress. IEEE Transactions on Power Electronics, 33(3), 2531–2551. doi: 10.1109/TPEL.2017.2690500

Degrenne, N., Ewanchuk, J., David, E., Boldyrjew, R., & Mollov, S. (2015). A review of prognostics and health management for power semiconductor modules.

Proceedings of the Annual Conference of the Prognostics and Health Management Society, PHM, 242–252.

Degrenne, N., & Mollov, S. (2018). On-line health monitoring of wire-bonded IGBT power modules using on-state voltage at zero-temperature-coefficient. PCIM Europe Conference Proceedings, (225809), 699–705.

Degrenne, N., & Mollov, S. (2019). Robust On-line Junction Temperature Estimation of IGBT Power Modules based on von during PWM Power Cycling. In 2019 IEEE International Workshop on Integrated Power Packaging, IWIPP 2019. doi: 10.1109/IWIPP.2019.8799086

Degrenne, N., Kawahara, C., & Mollov, S. (2019). A prognostics framework for power semiconductor IGBT modules through monitoring of the on-state voltage. Proceedings of the Annual Conference of the Prognostics and Health Management Society, PHM, 11(1), 1–9. doi: 10.36001/phmconf.2019.v11i1.829

Denk, M., & Bakran, M. M. (2015). Junction temperature measurement during inverter operation using a TJ-IGBT-Driver. PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings Of, (May), 19–21.

Denk, M., & Bakran, M. M. (2017). IGBT gate driver with accurate measurement of junction temperature and inverter output current. PCIM Europe 2017 - International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, (May), 16–18. doi: 10.1109/SBMicro.2017.7990693

Du, X., Li, T., Zhang, J., Tai, H. M., Sun, P., & Zhou, L. (2016). Thermal network parameter identification of IGBT module based on the cooling curve of junction temperature. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2016-May, 2992–2997. doi: 10.1109/APEC.2016.7468289

Dusmez, S., Ali, S. H., Heydarzadeh, M., Kamath, A. S., Duran, H., & Akin, B. (2017). Aging precursor identification and lifetime estimation for thermally aged discrete package silicon power switches. IEEE Transactions on Industry Applications. doi: 10.1109/TIA.2016.2603144

Eleffendi, M. A., & Johnson, C. M. (2017). In-Service Diagnostics for Wire-Bond Lift-off and Solder Fatigue of Power Semiconductor Packages. IEEE Transactions on Power Electronics, 32(9), 7187–7198. doi: 10.1109/TPEL.2016.2628705

Falck, J., Felgemacher, C., Rojko, A., Liserre, M., & Zacharias, P. (2018). Reliability of Power Electronic Systems. IEEE Industrial Electronics Magazine, 12(2), 24–35. doi: 10.1109/MIE.2018.2825481

Ghimire, P., Pedersen, K. B., Rannestad, B., & Munk-Nielsen, S. (2015). Ageing monitoring in IGBT module under sinusoidal loading. Microelectronics Reliability, 55(9–10), 1945–1949. doi: 10.1016/j.microrel.2015.06.025

Gonzalez-Hernando, F., San-Sebastian, J., Garcia-Bediaga, A., Arias, M., Iannuzzo, F., & Blaabjerg, F. (2018). Online Condition Monitoring of Bond Wire Degradation in Inverter Operation. ECCE 2018 - IEEE Energy Conversion Congress and Exposition. doi: 10.1109/ECCE.2018.8558460

Gonzalez-Hernando, F., San-Sebastian, J., Garcia-Bediaga, A., Arias, M., Iannuzzo, F., & Blaabjerg, F. (2019). Wear-Out Condition Monitoring of IGBT and mosfet Power Modules in Inverter Operation. IEEE Transactions on Industry Applications, 55(6), 6184–6192. doi: 10.1109/TIA.2019.2935985

GopiReddy, L. R., Tolbert, L. M., & Ozpineci, B. (2015). Power cycle testing of power switches: A literature survey. *IEEE Transactions on Power Electronics*, *30*(5), 2465–2473. doi: 10.1109/TPEL.2014.2359015

Griffo, A., Wang, J., Colombage, K., & Kamel, T. (2018). Real-time measurement of temperature sensitive electrical parameters in SiC power mosfets. IEEE Transactions on Industrial Electronics, 65(3), 2663–2671. doi: 10.1109/TIE.2017.2739687

Gutierrez, E., Lin, K., DeVoto, D., & McCluskey, P. (2019). Thermal assessment and in-situ monitoring of insulated gate bipolar transistors in power electronic modules. ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, InterPACK 2019, (February 2020). doi: 10.1115/IPACK2019-6470

Hu, Z., Du, M., & Wei, K. (2017). Online Calculation of the Increase in Thermal Resistance Caused by Solder Fatigue for IGBT Modules. IEEE Transactions on Device and Materials Reliability, 17(4), 785–794. doi: 10.1109/TDMR.2017.2746571

Hu, Z., Ge, X., Xie, D., Zhang, Y., Yao, B., Dai, J., & Yang, F. (2019). An aging-degree evaluation method for IGBT bond wire with online multivariate monitoring. Energies, 12(20). doi: 10.3390/en12203962

Hu, K., Liu, Z., Yang, Y., Iannuzzo, F., & Blaabjerg, F. (2020). Ensuring a Reliable Operation of Two-Level IGBT-Based Power Converters: A Review of Monitoring and Fault-Tolerant Approaches. IEEE Access, 8, 89988–90022. doi: 10.1109/ACCESS.2020.2994368

Huang, Y., Luo, Y., Xiao, F., & Liu, B. (2019). Failure Mechanism of Die-Attach Solder Joints in IGBT Modules under Pulse High-Current Power Cycling. IEEE Journal of Emerging and Selected Topics in Power Electronics, 7(1), 99–107. doi: 10.1109/JESTPE.2018.2871474

Ibrahim, A., Khatir, Z., Ousten, J., Lallemand, R., Degrenne, N., & Ingrossi D. (2020). Using of Bond-Wire Resistance as Ageing Indicator of Semiconductor Power Modules. ESREF 2020, 31st European

Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Oct 2020, Athènes, Greece. doi: 10.1016/j.microrel.2020.113757 . hal-03153283

Kexin, W., Mingxing, D., Linlin, X., & Jian, L. (2014). Study of bonding wire failure effects on external measurable signals of IGBT module. IEEE Transactions on Device and Materials Reliability. doi: 10.1109/TDMR.2012.2200485

Kong, Q., Du, M., Ouyang, Z., Wei, K., & Hurley, W. G. (2019). A method to monitor IGBT module bond wire failure using on-state voltage separation strategy. Energies, 12(9). doi: 10.3390/en12091791

Kuhn, H., & Mertens, A. (2009). On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters. 2009 13th European Conference on Power Electronics and Applications, EPE '09.

Li, L., Ning, P., Wen, X., Li, Y., Ge, Q., Zhang, D., & Tai, X. (2017). A turn-off delay time measurement and junction temperature estimation method for IGBT. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2290–2296. doi: 10.1109/APEC.2017.7931019

Liu, J., Zhang, G., Chen, Q., Qi, L., Qin, Z., Wang, J., & Geng, Y. (2018). Online junction temperature extraction and aging detection of IGBT via Miller plateau width. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2018-March, 2813–2820. doi: 10.1109/APEC.2018.8341416

Liu, J., Zhang, G., Chen, Q., Qi, L., Geng, Y., & Wang, J. (2019). In situ Condition Monitoring of IGBTs Based on the Miller Plateau Duration. IEEE Transactions on Power Electronics, 34(1), 769–782. doi: 10.1109/TPEL.2018.2820700

Luo, H., Chen, Y., Sun, P., Li, W., & He, X. (2016). Junction Temperature Extraction Approach with Turn-Off Delay Time for High-Voltage High-Power IGBT Modules. IEEE Transactions on Power Electronics, 31(7), 5122–5132. doi: 10.1109/TPEL.2015.2481465

Mandeya, R., Chen, C., Pickert, V., & Naayagi, R. T. (2018). Prethreshold Voltage as a Low-Component Count Temperature Sensitive Electrical Parameter Without Self-Heating. IEEE Transactions on Power Electronics, 33(4), 2787–2791. doi: 10.1109/TPEL.2017.2749179

Mandeya, R., Chen, C., Pickert, V., Naayagi, R.T., & Ji, B. (2019). Gate-emitter Pre-threshold Voltage as a Health Sensitive Parameter for IGBT Chip Failure Monitoring in High Voltage Multichip IGBT Power Modules. IEEE Trans. Power Electron, (35), 9158–9169. doi: 10.1109/TPEL.2018.2884276.

Mandeya, M. R. (2019). In-situ Health Monitoring Applied to High-Voltage IGBT Power Modules A thesis submitted for the degree of Doctor of Philosophy.

Nguyen, M. H., & Kwak, S. (2020). Enhance reliability of semiconductor devices in power converters. Electronics (Switzerland), 9(12), 1–37. doi: 10.3390/electronics9122068

Patil, N., Celaya, J., Das, D., Goebel, K., & Pecht, M. (2009). Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics. IEEE Transactions on Reliability, 58(2), 271–276. doi: 10.1109/TR.2009.2020134

Pedersen, K. B., Kristensen, P. K., Popok, V., & Pedersen, K. (2015). Degradation assessment in IGBT modules using four-point probing approach. IEEE Transactions on Power Electronics, 30(5), 2405–2412. doi: 10.1109/TPEL.2014.2344174

Peng, Y., Sun, P., Zhou, L., Du, X., & Cai, J. (2017). A temperature-independent method for monitoring the degradation of bond wires in IGBT modules based on transfer characteristics. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 1, 751–755. doi: 10.1109/APEC.2017.7930778

Mohamed Sathik, M. H., Prasanth, S., Sasongko, F., & Pou, J. (2018). Online condition monitoring of IGBT modules using voltage change rate identification. Microelectronics Reliability, 88–90(October), 486–492. doi: 10.1016/j.microrel.2018.07.040

Mohamed Sathik, M. H., Prasanth, S., Sasongko, F., & Pou, J. (2019). Online condition monitoring of IGBT modules using current-change rate identification. Microelectronics Reliability, 92(October 2018), 55–62. doi: 10.1016/j.microrel.2018.11.013

Schubert, M., & De Doncker, R. W. (2020). Semiconductor Temperature and Condition Monitoring Using Gate-Driver-Integrated Inverter Output Voltage Measurement. IEEE Transactions on Industry Applications, 56(3), 2894–2902. doi: 10.1109/TIA.2020.2977875

Singh, A., Anurag, A., & Anand, S. (2017). Evaluation of Vce at inflection point for monitoring bond wire degradation in discrete packaged IGBTs. IEEE Transactions on Power Electronics, 32(4), 2481–2484. doi: 10.1109/TPEL.2016.2621757

Smet, V., Forest, F., Huselstein, J. J., Richardeau, F., Khatir, Z., Lefebvre, S., & Berkani, M. (2011). Ageing and failure modes of IGBT modules in high-temperature power cycling. IEEE Transactions on Industrial Electronics, 58(10), 4931–4941. doi: 10.1109/TIE.2011.2114313

Sun, P., Gong, C., Du, X., Peng, Y., Wang, B., & Zhou, L. (2017a). Condition Monitoring IGBT Module Bond Wires Fatigue Using Short-Circuit Current Identification. IEEE Transactions on Power Electronics, 32(5), 3777–3786. doi: 10.1109/TPEL.2016.2585669

Sun, P., Gong, C., Du, X., Luo, Q., Wang, H., & Zhou, L. (2017b). Online Condition Monitoring for Both IGBT

Module and DC-Link Capacitor of Power Converter Based on Short-Circuit Current Simultaneously. IEEE Transactions on Industrial Electronics, 64(5), 3662–3671. doi: 10.1109/TIE.2017.2652372

Sundaramoorthy, V. K., Bianda, E., Bloch, R., & Zurfluh, F. (2014). Simultaneous online estimation of junction temperature and current of IGBTs using emitter-auxiliary emitter parasitic inductance. PCIM Europe Conference Proceedings, (May 2014), 690–697.

Tian, B., Qiao, W., Wang, Z., Gachovska, T., & Hudgins, J. L. (2014). Monitoring IGBT's health condition via junction temperature variations. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2550–2555. doi: 10.1109/APEC.2014.6803662

Tsukuda, M., Guan, L., Watanabe, K., Yamaguchi, H., Takao, K., & Omura, I. (2020). V-I Curve Based Condition Monitoring System for Power Devices. Proceedings of the International Symposium on Power Semiconductor Devices and ICs, 2020-September, 82–85. doi: 10.1109/ISPSD46842.2020.9170059

Van Der Broeck, C. H., Gospodinov, A., & De Doncker, R. W. (2018). IGBT Junction Temperature Estimation via Gate Voltage Plateau Sensing. IEEE Transactions on Industry Applications, 54(5), 4752–4763. doi: 10.1109/TIA.2018.2836362

Wang, C., He, Y., Wang, C., Li, L., & Wu, X. (2020). Multi-chip IGBT module failure monitoring based on module transconductance with temperature calibration. Electronics (Switzerland), 9(10), 1–17. doi: 10.3390/electronics9101559

Wang, Z., Tian, B., Qiao, W., & Qu, L. (2016). Real-Time Aging Monitoring for IGBT Modules Using Case Temperature. IEEE Transactions on Industrial Electronics, 63(2), 1168–1178. doi: 10.1109/TIE.2015.2497665

Wang, B., Cai, J., Du, X., & Zhou, L. (2017). Review of Power Semiconductor Device Reliability for Power Converters. CPSS Transactions on Power Electronics and Applications, 2(2), 101–117. doi: 10.24295/cpsstpea.2017.00011

Wang, K., Zhou, L., Sun, P., & Du, X. (2020). Monitoring Bond Wires Defects of IGBT Module Using Module Transconductance. IEEE Journal of Emerging and Selected Topics in Power Electronics, 6777(c), 1–1. doi: 10.1109/jestpe.2020.2973348

Wu, R., Blaabjerg, F., Wang, H., Liserre, M., & Iannuzzo, F. (2013). Catastrophic failure and fault-tolerant design of IGBT power electronic converters - An overview. In IECON Proceedings (Industrial Electronics Conference). doi: 10.1109/IECON.2013.6699187

Yang, S., Xiang, D., Bryant, A., Mawby, P., Ran, L., & Tavner, P. (2010) "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," in *IEEE Transactions on Power Electronics*, 25(11), 2734-2752. doi: 10.1109/TPEL.2010.2049377.

Ye, X., Chen, C., Wang, Y., Zhai, G., & Vachtsevanos, G. J. (2017). Online Condition Monitoring of Power MOSFET Gate Oxide Degradation Based on Miller Platform Voltage. IEEE Transactions on Power Electronics, 32(6), 4776–4784. doi: 10.1109/TPEL.2016.2602323

Zhang, J., Du, X., Zheng, S., & Tai, H. M. (2018). Thermal resistor and capacitor parameter identification using cooling curve of IGBT module. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2018-March, 1729–1733. doi: 10.1109/APEC.2018.8341251

Zhang, J., Du, X., Yu, Y., Zheng, S., Sun, P., & Tai, H. M. (2019a). Thermal parameter monitoring of IGBT module using junction temperature cooling curves. IEEE Transactions on Industrial Electronics, 66(10), 8148–8160. doi: 10.1109/TIE.2018.2883258

Zhang, J., Du, M., Jing, L., Wei, K., & Hurley, W. G. (2019b). IGBT Junction Temperature Measurements: Inclusive of Dynamic Thermal Parameters. IEEE Transactions on Device and Materials Reliability. doi: 10.1109/TDMR.2019.2910182

Zhang, Z., Dyer, J., Wu, X., Wang, F., Costinett, D., Tolbert, L. M., & Blalock, B. J. (2019). Online Junction Temperature Monitoring Using Intelligent Gate Drive for SiC Power Devices. IEEE Transactions on Power Electronics, 34(8), 7922–7932. doi: 10.1109/TPEL.2018.2879511

Zhou, S., Zhou, L., & Sun, P. (2013). Monitoring potential defects in an IGBT module based on dynamic changes of the gate current. IEEE Transactions on Power Electronics, 28(3), 1479–1487. doi: 10.1109/TPEL.2012.2210249