# A Review of Prognostics and Health Management for Power Semiconductor Modules

Nicolas Degrenne[1], Jeffrey Ewanchuk, Erwan David, Roman Boldyrjew and Stefan Mollov

*Mitsubishi Electric R&D Centre Europe, Rennes, 35708, France*

[1]*n.degrenne@fr.merce.mee.com*

## ABSTRACT

In this paper, a review of current techniques used in the prognostics and state-of-health monitoring for power semiconductor modules is provided. Given the increasing trend in power modules having a larger share of the power electronic market, understanding their lifetime limitations is critical to improving the life-cycle cost of the power electronic product. Hence, this paper reviews common failure mechanisms in power modules and the state-of-art in predicting the lifetime of the module based on a given mission profile. Prognostics are reviewed in terms of stress-based and condition monitoring-based methods, while the potential of prognostics is presented for applications that utilize power modules.

## 1. INTRODUCTION

Owing to their lowered parasitic construction, high performance and relatively low manufacturing effort, power semiconductor modules are often preferred in applications where the power exceeds a few kilo-watts. This preference in higher power applications can be further appreciated by the fact that lower cost dies can be easily paralleled within a single power module to increase the rating of that module without having to manufacture a single large power die (Wintrich, Nicolai, Tursky & Reimann, 2011). Hence, since 2008, the market size for power modules occupies a larger proportion of the total market for power electronic devices - with a predicted market share of 30% by 2020 (Madjour, 2014).

Power modules are constructed with several mechanical layers, as seen in Figure 1. Commonly, the die is attached to a DBC (direct bonded copper), via solder, that is composed of a bonded copper-ceramic-copper structure, allowing electrical isolation but with high thermal conductivity towards the heatsink. In order to mate the DBC with the heatsink and increase the thermal capacity of the system, a

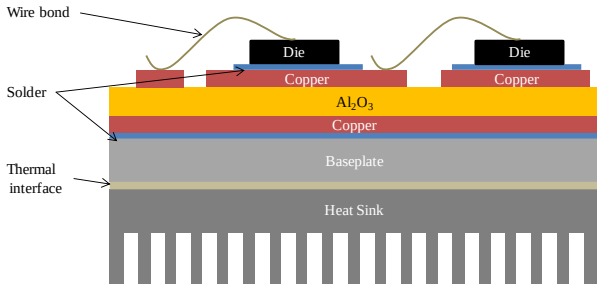


Figure 1. Power Module used in a Power Electronic Converter (shown without encapsulation and casing)

base-plate is also typically used in medium and high power modules (Wintrich et al. 2011).

Furthermore, using a thermally conductive interface material, the module (base-plate-DBC-die) is attached to the heatsink, completing the thermal extraction path. In this paper, the presence of these layers within the power module is a critical aspect for determining its lifetime.

Depending on the application of a power converter, the power devices and the capacitors can exceed half the reported failures - with power devices being the largest single component (Yang, Bryant, Mawby, Xiang, Ran & Tavner, 2011). These failures are typically a result of environmental factors, overload conditions, and system transients (Yang et al. 2011). Hence, in difficult-to-service applications such as off-shore wind converters, there is an increasing amount of pressure to predict maintenance intervals and improve replacement costs by studying the reliability of power modules, (Ma, Liserre, Blaabjerg, & Kerekes, 2014). These same techniques have also found their way into automotive applications, where the application conditions vary widely and the reliability of the converter is less deterministic (Hirschmann, Tissen, Schröder & De Doncker, 2007). In both applications, the total lifecycle cost of the converter can be decreased with proper prediction of the lifetime. Hence, this paper provides a review of prognostic and health management techniques

for power modules, with the aim of predicting the remaining useful life of the power module, as illustrated in figure 2.

As the chief aim of the paper is to review the methods relevant to lifetime prediction of power modules, section 2 of this paper covers the failure mechanisms present in typical IGBT-based power modules. In section 3, mission profile based lifetime estimation techniques are presented, with stress-based and condition monitoring-based prognostic methods highlighted in sections 4 and 5 respectively. Finally, section 6 details some potential applications for prognostics in power modules.

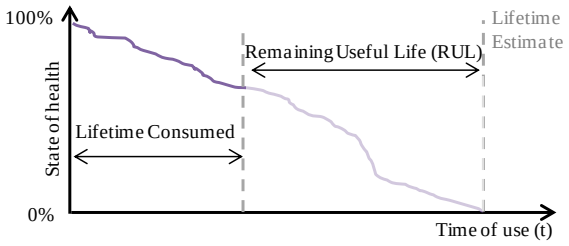


Figure 2. Remaining useful lifetime of a power module

## 2. FAILURE MECHANISMS

The aging of devices is caused by different material properties of adjacent layers, as shown in Figure 1, specifically due to the different coefficients of thermal expansion (CTE) leading to a bimetal-like effect. Hence, during heat-up and cool-down phases the dissimilar expansion of adjacent layers causes a shear stress along the contact surface. Two principal failure mechanisms have been identified to be responsible for wear: bond wire lift-off and solder fatigue (Lutz, Schlangenotto, Scheuermann & De Donker, 2011) (Fig. 3). Reconstruction of metallization is mentioned in the literature as a third failure mechanism but it is not completely investigated yet (Lutz et al. 2011), (Wu, Held, Jacob, Scacco & Birolini, 1995), (Wintrich et al. 2011).

### 2.1. Bond wire lift-off

Bond wire is a cost-effective process to make an interconnection with the source, on the top of the die. Usually, bond wires are made of Al and have therefore a higher CTE value than Si dies. Hence bond wires expand more than the connected chip. As a consequence wires themselves are under stress caused by bending and the interface between bond and chip is under shear stress (Wintrich et al. 2011).

Degradation starts usually at the edges of the interface and is presented as crack growth. The cracks generally spread around grain boundaries above the interface, in the wire bond. A reasonable explanation for this is that a softening and hardening occurs during the bonding process, leading to

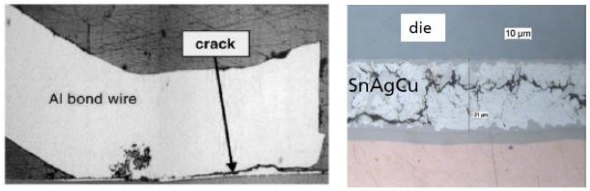


Figure 3. Bond wire (left) and solder (right) cracks. Pictures from ECPE workshop on "reliability and lifetime estimation", 2013.

a higher reliability of the interconnection and a reduced reliability of the bond wire itself (Onuki, Koizumi & Suwa, 2000). Cracks grow towards the center of the interconnection, decreasing the contact area. Therefore the electrical resistance is increasing, measurable as a growing of forward voltage drop. Consequently, the power losses rise up leading to a higher junction temperature during power-on time. Eventually higher thermo-mechanical stress will finally lead to a bond wire lift-off. A single lift-off will accelerate the degradation process, because the full load current will increase the current per bond for the remaining wires leading to higher temperature at the interconnection (Goehre, Schneider-Ramelow, Geißler & Lang, 2010), (Lutz et al. 2011), (Onuki et al. 2000), (Bayerer, Herrmann, Licht, Lutz & Feller, 2008). The last bond wire carrying the highest current density typically leaves a crater just under its heel after lifting-off. Such a crater is usually a characteristic of an arc flash-over (Lutz et al. 2011). The lifetime of bond wires has increased lately thanks to better bond alloys, improved bonding technology and optimization of the bond wire geometry (Amro, Lutz, Rudzki, Sittin & Thoben, 2006).

### 2.2. Solder delamination

Solder fatigue is the second most common aging mechanism in power modules. In popular semiconductor power modules there are two solder layers where solder fatigue occurs: within the solder between base-plate and DBC or chip and DBC. Stresses cause fractures formation inside the solder interfaces. With Pb-based solders, delamination starts usually in the edges and corners of the layer and is spreading towards centre. The thermal impedance is increased, thereby raising the junction temperature of the die. In this manner, higher thermo-mechanical stress accelerates the aging in a positive feedback loop (Lutz et al. 2011). During the last couple of years, Pb-free solder layers were investigated (Morozumi, Yamada, Miyasaka, Sumi & Seki, 2003), (Herrmann, Feller, Lutz, Bayerer & Licht, 2007). It was shown that with Sn/Ag solder, cracks originate in the center and spread in vertical and reticulated structures at tin grain boundary. It was also shown that Pb-free solder layers lead to higher reliability even if bond wires haven't been improved (Hensler, Lutz, Thoben & Guth, 2010), indicating a cross-coupling reliability effect between the top- and bottom-side die terminations.

The aging of solder joints can be detected by scanning acoustic microscopy (SAM) and by calculating thermal resistance during the test. Usually, the end-of-life criterion from semiconductor power modules is reached when the thermal resistance has increased by more the 20% (Hensler et al. 2010).

## 3. MISSION PROFILE BASED LIFETIME ESTIMATION

Design for reliability consists in designing a power module not only with respect to functional requirements but also to reliability requirements (Lu, Bailey & Yin, 2009). It requires estimating lifetime of the module under study, usually with minimum reliability figure in mind

The lifetime estimation is generally obtained with a stepwise approach (Mainka, Thoben & Schilling 2011) from an estimation of the usage (mission profile). It employs an electrical, thermal and damage model of the Device Under Test (DUT) (Fig. 4). This approach assumes that the device will be used according to the pre-defined mission profile, and that the device assembly will endure a known number of stress cycles (Fig. 5), an assumption that is difficult to fulfill in reality.

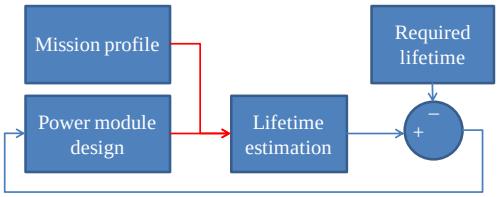


Figure 4. Design for reliability

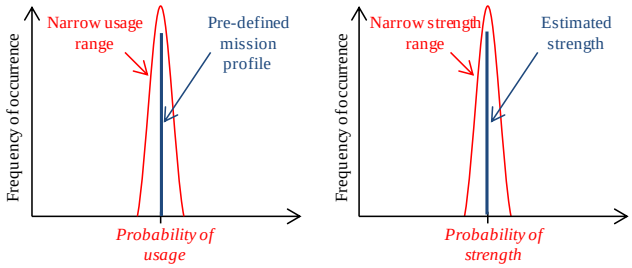


Figure 5. Mission profile-based methods can be used in applications where usage is well identified

### 3.1. From mission profile to junction temperature profile

A number of application-specific mission profiles have been defined. Solar radiation profiles are used in photovoltaic applications (Yang, Wang & Blaabjerg 2015), wind profiles in wind power applications (Ma et al. 2014), sea elevation profiles for direct wave energy converter (Kovaltchouk, Aubry, Multon & Ben Ahmed, 2013 ) or drive cycle for automotive domain as detailed below.

A mission profile in automotive application can be derived from a speed profile representative of the average driving style. A collection of driving styles corresponding to different types of driving categories is available in the literature (Barlow, Latham, Mccrae & Boulter 2009) such as FTP-72 (Hirschmann, Member, Tissen, Schröder & Doncker, 2007) or NEDC (Biela, Waffler, & Kolar, 2009) as shown in Fig. 6.

The loss profile of each die in the power module is translated from the mission profile by considering traction chain characteristics and various parameters related to the motor and the converter (Thoben, 2008). A thermal model is then applied and results in a junction temperature profile $T_J$ (Lu et al., 2009)(Fig. 6). Note that $T_J$ is fed back in the calculation of the power losses.

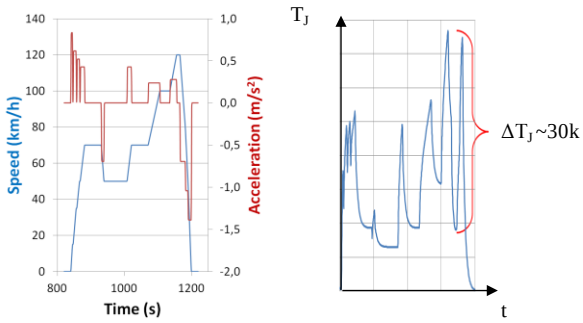


Figure 6. NEDC driving cycle (left) (blue: speed, red:

### 3.2. From junction temperature profile to lifetime estimation

A counting method is used to extract and classify the thermal cycles. The rainflow algorithm is able to capture compound temperature variations, and is considered to be amongst the better performing algorithms (Mainka et al. 2011).

The stresses are converted into damage with a damage model. This model is either derived from physical models (Kovacevic, Drofenik & Kolar, 2010) or with data-driven approach using power cycling tests (Scheuermann & Schmidt, 1997). Different models are commonly used such as Coffin-Manson (Halford & Manson, 1967), LESIT (Held, Jacob, Nicoletti, Scacco & Poech, 1997), CIPS08 (Bayerer, Hermann, Licht, Lutz & Feller, 2008),

The damages are then summed using Palmgren-Miner linear accumulation rule (Miner, 1945), though this is increasingly questioned (Aal, 2014). In (Huang & Mawby, 2013), the damage level is fed-back to the thermal model. The lifetime is calculated based on the duration of the mission profile and the corresponding computed damage. Based on the lifetime estimation, the design can be adjusted to meet the reliability requirements.

## 4. STRESS-BASED PROGNOSTICS

Analyzing a pre-defined mission profile provides insight into potential reliability problems that may or may not develop during the life of a product. Although such insight is beneficial during the design and the operational phases of the product, the information quickly becomes obsolete once the product usage (e.g. operating and environmental characteristics) deviates significantly from the assumed operating conditions that have been originally analysed. That is why monitoring of real-life operating and environmental conditions is used to derive the reliability problems based on the actual operating and environmental conditions.

Stress-based methods quantify the cause of degradation: stress (Fig. 7). They are most adequate when the manufacturing process deviations (i.e. strength range) are narrow and when the usage cannot be easily pre-defined or has large deviations (Fig. 8).

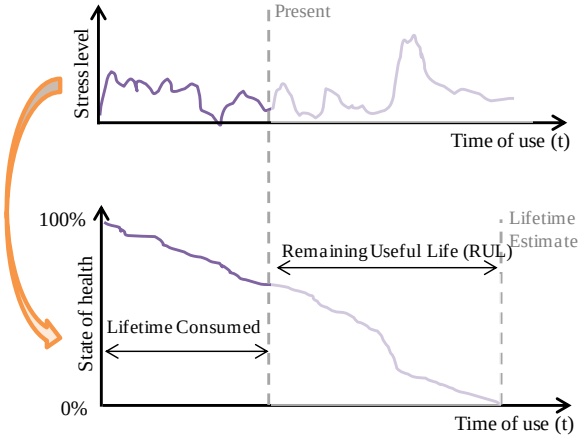


Figure 7. RUL estimation based on Stress

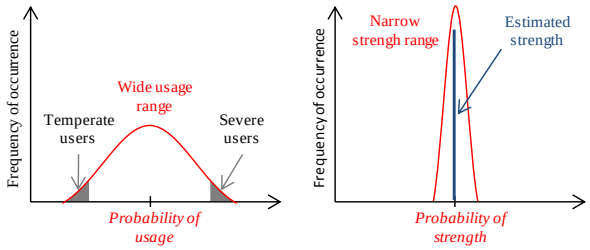


Figure 8. Stress-based methods can be used in applications where usage is not well identified

In order to estimate the stress, the methods relying on power and thermal models (as presented in section 3) can be implemented in real-time. Alternatively, the junction temperature $T_J$ can be measured on-line. Then, the stress is quantified with a real-time algorithm and converted to a State-of-Health (SoH). The SoH is extrapolated to estimate the End-of-Life (EoL) and the Remaining Useful Life (RUL).

### 4.1. Junction temperature measurement

A first approach is to position a conventional thermal sensor in the vicinity of the power chip. Commercially available negative temperature coefficient (NTC) thermistors operate up to 200°C, and can be attached with standard processes (e.g. sintering, wire-bonding). This approach measures the temperature several millimeters away from the junction, and has a low space and time resolution, the relevance of the provided information is thus questionable.

A second approach is to create a temperature sensor on the silicon power die itself. In a patent, Schuler (2011) develops the idea of a thermocouple circuit formed by two bonding wires and a pad to measure the temperature difference between the chip and the carrier. In (Motto & Donlon 2012), a string of diodes is fabricated on the IGBT chip's surface (Fig. 9). The linear dependence of the forward voltage drop is used to estimate temperature. This solution has the required performance but is not cost-effective as it occupies a valuable real estate on the power die.

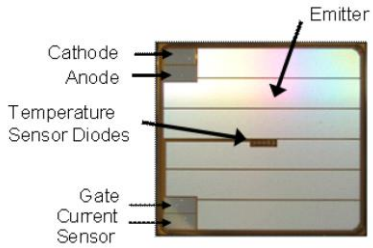


Figure 9. IGBT chip current and temperature sensors (Motto et al. 2012)

A third approach is to monitor Thermo-Sensitive Electrical Parameters (TSEP), inherent to the semiconductor device (Avenas, Dupont & Khatir, 2012), (Baker, Liserre, Dupont & Avenas, 2014). Some TSEPs such as voltage drop at low current and saturation current have to be done in specific electrical conditions and often necessitate an alteration to the structure or operation of a power electronic converter. Table 1 compares methods that can be performed online, either during the conduction time or the switching time. All these methods require accurate sensors and chip-level calibration. They must be compared in terms of linearity, dependence in operating conditions outside of temperature, sensitivity and implementation cost. Converter-level methods such as low-order harmonics identification in an inverter (Xiang, Ran, Tavner, Yang, Bryant & Mawby, 2012) are not included in the table.

Table 1. On-line TSEP-based methods not requiring alteration of the converter.

| TSEP | Reference | Description |
|---|---|---|
| Voltage at high current of transistors and diodes | (Kim & Sul, 1998)<br>(Perpiñà, Serviere & Saiz, 2006)<br>(Koenig & Plum, 2007)<br>(Lutz, Paul & Zill, 2011)<br>(Dupont, Avenas & Jeannin 2013) | Requires very accurate sensors and high-voltage protection. Sensitivity of approx. 20mV/°C. Measurement influenced greatly by parasitic elements inside power modules (bond wires, etc.), and load current. Is also a DSEP (Table 2). |
| Turn-off transition time of IGBT transistors | (Barlini & Ciappa, 2006)<br>(Kuhn & Mertens, 2009)<br>(Bryant, Yang, Mawby, Xiang, Ran, Tavner & Palmer, 2011)<br>(Xu, Jiang, Li & Ning, 2013) | Sensitivity of approx. 2ns/K. Changes have also been viewed in harmonics in the output of an IGBT inverter. |
| Turn-on delay and/or di/dt of transistors | (Barlini & Ciappa, 2007)<br>(Kuhn & Mertens, 2009)<br>(Sundaramoorthy, Bianda, Bloch & Zurfluh, 2014) | Increase in gate resistance during the measurement is proposed to slow down the process. Sensitivity of approx. 2ns/K or 40A/(µs.K) for high power IGBTs. |
| Threshold voltage of MOS transistors | (Chen, Pickert, Atkinson & Pritchard, 2006)<br>(Bahun, Sunde & Jakopovic, 2013) | The sensing circuit can be implemented in the gate driver. The threshold voltage is measured when the current starts flowing through the transistor. Sensitivity of approx. 10mV/K. |
| Gate parasitic (internal resistance and capacitances) | (Sundaramoorthy, Bianda, Bloch, Nistor, Knapp & Heinemann, 2013)<br>(Baker, Munk-Nielsen, Liserre & Iannuzzo, 2014)<br>(Niu & Lorenz, 2014)<br>(Niu&Lorenz, 2015) | The sensing circuit can be implemented in the gate driver. The sensed parameter can either be the duration of the Miller plateau phase (approx. 1.2ns/K), the voltage during turn-on delay (approx. 20mV/K), the gate charge (approx. 250pC/K) or the gate current transient such as the peak current (approx. 2.5mA/K). |

### 4.2. Real-time stress-counting algorithms

The rainflow algorithm traditionally uses the entire time history of the junction temperature. This approach is inconvenient in real-time applications because the algorithm must be applied periodically to large datasets. A first option is to use the rainflow algorithm on windows of data of e.g. 1 day in order to reduce the size of the dataset. A second option is to use another type of stress-counting algorithm. Three alternative real-time stress-counting algorithms are evaluated with respect to wire-bond and chip solder failures in (Mainka et al. 2011). The rising edge and half-cycle methods process each minima and maxima value as it occurs and give acceptable results. An on-line stress-couting algorithm is used in (Musallam, Johnson, Yin, Bailey & Mermet-Guyennet, 2010) and (James 2012), but the performances of the algorithms are not evaluated experimentally.

### 4.3. State-of-Health extrapolation

The time history of the state of health is required to determine the RUL of a device. It is linearly extrapolated according to the following equation (Fig. 10):

$$RUL_n = \frac{n \times SoH_n}{100 - SoH_n}$$

with *n* the time variable, *SoH* the state of health (in %).

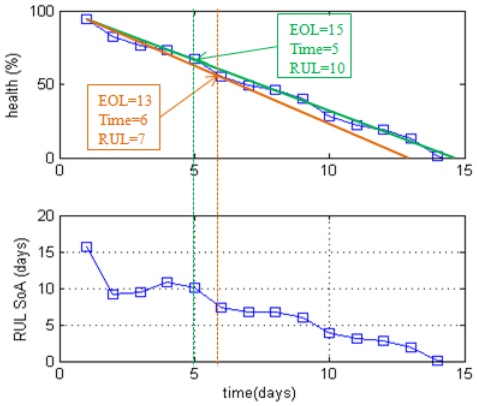


Figure 10. State-of-Health linear extrapolation to estimate EoL and RUL.

## 5. CONDITION-MONITORING PROGNOSTICS

Unlike stress-based methods, condition-monitoring (CM) methods examine the consequence of degradation, i.e. the evolution in time of one or several Damage-Sensitive Electrical Parameters (DSEP), also mentioned as failure precursors (Fig. 11). As such, CM methods are useful in applications where devices present variations due to manufacturing process dispersion (Fig. 12).

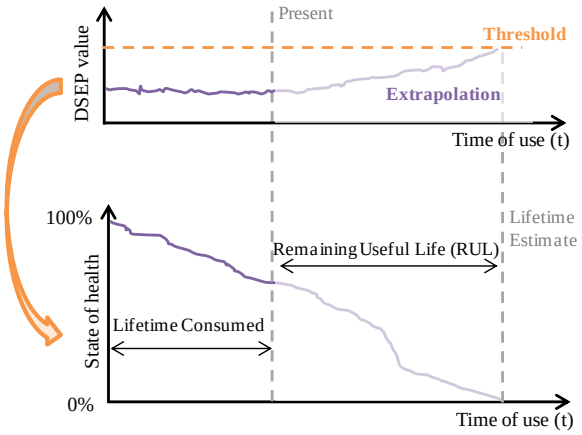


Figure 11. RUL estimation based on Damage-Sensitive Electro Parameter (DSEP)

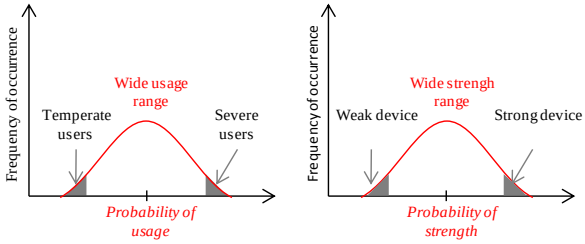


Figure 12. Condition monitoring can be used in applications where usage and/or strength is not well identified.

The selection of a DSEP depends on the preferred failure mode and on the ease of implementation. In order to convert the deviation of the DSEP into a RUL estimate, a threshold value is determined, and the time deviation is extrapolated (Fig. 11). Two approaches are opposed in the literature: (a) past-history approaches that only use past DSEP data on the DUT itself, and (b) model-based approaches that use data from other devices to generate a model.

### 5.1. Damage Sensitive Electrical Parameters

Table 2 sums up the DSEP parameters that have been treated and reviewed (Yang, Xiang, Bryant, Mawby, Ran & Tavner, 2010) in the literature. In the case of solder degradation, all methods discussed in paragraph 3.1 to estimate the junction temperature are useful to estimate the value of $R_{TH}$. In the case of wire-bond failure (lift-off), the electrical path is suddenly degraded, and the voltage at high current experiences an abrupt, distinguishable increase. $T_J$ increases as well, as a consequence to the loss increase. In order to isolate the impact of bond-wire degradation from solder-crack degradation, the impact of temperature on the voltage can be compensated (Rashed, Forest, Huselstein, Martire & Enrici, 2013), (Ji, Pickert, Cao & Zahawi, 2013).

Note that on-line measurement may not be a requirement anymore for CM since it is possible to monitor health discontinuously, before or after the operation of the converter. In his thesis, Ji (2011) performs wire-bond and solder condition monitoring of an automotive inverter employing a calibrated operating point sequence taking approx. 5s. However, applications permitting such calibration procedures are rare in practice.

### 5.2. DUT past-history approach

The prognostic algorithm only uses the past history of the device to estimate its health and the RUL. The extrapolation typically uses a regression framework based on either statistical or Markov chains.

In (Celaya, Saxena, Saha, Vashchenko & Goebel, 2011), a Gaussian Process Regression (GPR) is used on discrete power MOSFETs. A distribution is tuned to fit available measurements, used to output a mean and covariance function, and to predict mean value and corresponding variance for a future point of interest (Fig. 13).

Past-history approach offers the advantage of requiring no training data set from other devices, even if domain knowledge is necessary to define the prior distribution and the type of covariance function. In (Celaya, Saxena, Saha & Goebel, 2011), the GPR method is compared to two model-based approaches discussed in the following section, and shown to be less efficient with respect to several prognostic performance metrics.

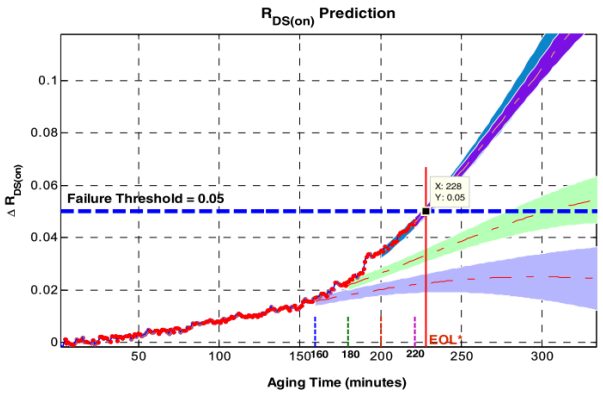


Figure 13. Prediction of RUL for aged device using GPR technique (Celaya, Saxena, Saha, Vashchenko & Goebel, 2011).

Table 2. Damage-Sensitive Electrical Parameters (DSEP)

| DSEP | Reference | Failure mechanism |
|---|---|---|
| $R_{TH}$ -based methods | (Ji, Song, Cao, Pickert, Hu, Mackersie & Pierce, 2014)<br>(Saha, Celaya, Wysocki & Goebel, 2009) | Chip solder<br>DBC solder |
| Voltage at high current | (Celaya, Saxena, Wysocki, Saha & Goebel, 2010)<br>(Ji, Pickert, Cao & Zahawi, 2013)<br>(Smet, Forest, Rached & Richardeau, 2012)<br>(Beczkowski, Ghimre, De Vega, Munk-Nielsen, Rannestad & Thogersen, 2013)<br>(Ghimire, De Vega, Munk-Nielsen, Rannestad & Thogersen 2013) | Wire-bond<br>Reconstruction of metalization |

### 5.3. Model-based approach

In the model-based approach, a training data set from other devices is used to model the evolution of the DSEP with time. The model can either be empirical or physical and is established after accelerated aging experiments on other devices and/or simulations. The prognostic algorithm uses the model and the measurements on the DUT to estimate the health and the RUL. Prognostic methods used in the literature are mainly Extended Kalman Filter (EKF) and Particle Filter (PF) (Baraldi, Maio & Zio, 2014).

In (Celaya, Saxena, Saha & Goebel, 2011), (Patil, Das & Pecht, 2012), and (Saha, Celaya, Vashchenko, mahiuddin & Goebel, 2011), several aged discrete devices are used to fit an empirical model of the evolution of $R_{DS-ON}$, $V_{CE-ON}$, and $V_{TH}$ respectively. The observations on the DUT are related to the empirical models with a particle filter to estimate the degradation state. In (Alghassi, Perinpanayagam & Samie, 2015), an alternative to EKF and PF is proposed. The $V_{CE-ON}$ value is decomposed into 9 discrete steps. A training dataset of 3 discrete IGBTs is used to provide a statistical distribution for the duration of each state. It is then used with Monte-Carlo simulations to investigate a statistical RUL prediction. The result is a light-weight simulation-based prognostic approach requiring only 0.3ms computation time for each measurement.

## 6. POTENTIAL OF PROGNOSTICS FOR POWER MODULES

The cost associated with the implementation of prognostic means in a power module has to be counterbalanced with quantifiable benefits. First, the prognostic information can be used in order to develop cost-optimized minimum-intervention and just-in-time maintenance strategies. Second, active health management can be employed to redistribute the stress to extend the life time of a device based on prognostic information.

### 6.1. Asset Management

Two asset-management strategies are commonly used in the field of power electronics: replacement after failure, and replacement at fixed intervals (in mission critical applications). Prognostic is a key enabler to asset management that ensures a good compromise between the risk of failure and the return on investment.

The development of a business model is necessary to support asset management. Return on investment calculations were applied to various electronic products (Sandborn & Wilkinson, 2007), (Feldman, 2009) and (Haddad, Sandborn & Pecht, 2014) but no business case was published for power modules until now. The main difficulty of establishing a business model is to estimate all costs additions (non-recurring, recurring, infrastructure) and cost avoidances (failure cost, maintenance cost) that are used by the stochastic simulator.

Manufacturers of power modules are facing problems to provide users with a year-based warranty. This is because of the considerable impact of system integration, operating and environmental conditions. Manufacturers would more easily provide a warranty based on applied stressors, such as number of junction temperature cycles.

### 6.2. Active stress reduction or redistribution

Stress reduction limits the performances of the system in order to extend the life time. The most straightforward implementation consists in de-rating (load current, operating voltage) of the module. This approach increases the system costs, and other solutions are preferred (Table 3). Several methods are commonly combined to offer various degrees of lifetime control. These methods can be used as a protection for over-temperature $T_{JMAX}$, and as a mean to decrease power cycling stress, reducing the $\Delta T_J$ around $T_{JMEAN}$ value. Another type of active control consists in controlling the minimum case temperature for the power module. Hence, as the fluctuations of junction temperature are reduced (Davidson, Stone & Foster, 2014) the lifetime of the module should increase, but no study was yet performed to evaluate CTE mismatch decrease and lifetime gain. Lastly, while the redistribution of stress between distinct power modules is not covered by this paper, some methods have been demonstrated for actively controlling parallel power modules (Hofer, Karrer and Gerster, 1996). However, it should be noted that for the latter method, the aim is to equalize the current distribution across the parallel set of modules, rather than to directly control the temperature to increase the lifetime of the module.

Table 3. Thermal and lifetime control techniques

| Parameter | Description | Downside | References |
|---|---|---|---|
| Load current | Decrease conduction losses | Load current decrease | (Blasko, Lukaszewski & Sladky, 1999)<br>(Murdock, Torres & Connors, 2006)<br>(Lemmens, Driesen & Vanassche, 2012) |
| Switching frequency | Decrease switching losses | Load ripple increase | (Blasko et al. 1999)<br>(Murdock et al. 2006)<br>(Lemmens et al. 2012)<br>(Weckert & Roth-Stielow, 2011)<br>(Wei, McGuire & Lukaszewski, 2011)<br>(Lo Calzo, Lidozzi, Solero, Crescimbini & Cardi, 2012) |
| DC-link voltage regulation | Decrease conduction losses | Oversized actives and passives, risk for random failures | (Andresen & Liserre, 2014) |
| Modulation strategy | Modify modulation type (continuous/discontinuous) or pattern | EMI difficult to control | (Lo Calzo et al. 2012)<br>(Ma & Blaabjerg, 2014) |
| Active gate driving | Increase the gate voltage | Potential gate oxide degradation | (Wu & Castellazzi 2010) |
| Heatsink | Increase cooling effort | Oversized cooling system<br>Efficacy not proven | (Law & Harley 2004)<br>(James, 2012)<br>(De Rijck & Huisman, 2013)<br>(Davidson et al. 2014) |

## 7. CONCLUSION

As a result of increasing market penetration of power modules, the motivation to better understand their lifetime and health is paramount to continuing this trend. Hence, this paper presented a review of prognostic methods, starting with failure mechanisms and continuing with methods of counting stress or directly measuring the state of health.

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