Effect of Electrostatic Discharge on Electrical Characteristics of Discrete Electronic Components (Technical Brief)

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ABSTRACT

This article reports on preliminary results of a study conducted to examine how temporary electrical overstress seed fault conditions in discrete power electronic components that cannot be detected with reliability tests but impact longevity of the device. These defects do not result in formal parametric failures per datasheet specifications, but result in substantial change in the electrical characteristics when compared with pristine device parameters. Tests were carried out on commercially available 600V IGBT devices using transmission line pulse (TLP) and system level ESD stress. It was hypothesized that the ESD causes local damage during the ESD discharge which may greatly accelerate degradation mechanisms and thus reduce the life of the components. This hypothesis was explored in simulation studies where different types of damage were imposed to different parts of the device. Experimental results agree qualitatively with the simulation for a number of tests which will motivate more in-depth modeling of the damage.

1. INTRODUCTION

Electronic components form an integral and critical part of on-board systems and are present in vehicle controls, communications, navigation, radar systems, etc. Future aircraft systems, including electric aircrafts and Unmanned Aerial Vehicles (UAVs), or the Next Generation Air Transportation Systems (NGATS), will certainly rely on more electric and electronic subsystems and components. The increase of new functionality will also increase the number of electronics faults with perhaps unanticipated fault modes. In addition, the move toward lead-free electronics and Micro-Electro-Mechanical Systems (MEMS) will further result in unknown anomalous behavior. To improve aircraft reliability, assure in-flight performance, and reduce maintenance costs, it is therefore imperative to provide system health awareness for digital electronics. To that end, an understanding of the behavior of deteriorated components is needed, as well as the capability to anticipate failures and predict the remaining life of embedded electronics is desired.

The development and advancement of this capability is also relevant to multiple NASA

Exploration Systems Mission Directorate (ESMD) vehicles, including the Orion, Ares, and future vehicles, such as the Lunar Surface Access Module (LSAM). In addition, there is relevance to long-endurance robotic space missions from ESMD and Space Mission Directorate (SMD).

Generally, an understanding of intrinsic and extrinsic degradation mechanisms of component level devices is crucial for the adoption and application of health management to systems. Within the field of electronics, knowledge of semiconductor degradation under various system and environmental scenarios may be coupled with prognostic algorithms to predict future state and time–to–failure of semiconductor components.

The existence of measurable extrinsic degradation precursors, pertaining to device packaging, has been well established in literature for power transistor devices. In recent literature, intrinsic degradation precursors related to the physical properties of the semiconductor, have also been observed. However, it is not widely known how degradation mechanisms propagate as a function of environmental conditions and various stressors. The attainment of such knowledge is critical for advancements in the field of power electronics health management and prognostics. Therefore, the ability to perform experiments on semiconductor devices for characterization of degradation precursors under various scenarios is of great interest.

Electrostatic discharge (ESD) is a major source of damage and failure of discrete electronic devices especially Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Integrated Gate Bipolar Transistor (IGBTs) which are extremely sensitive to such discharges. For most small devices, ESD can lead to immediate failure. For devices, such as power MOSFETs and IGBTs that are used for high-power applications, significant ESD levels are often required to cause complete failure. However, even smaller levels of ESD may stress the component which will lead to accelerated aging of the device. Thus, understanding ESD related damages and its effects on the aging of power electronics is of great significance. In this technical brief, we present our initial results and analysis of ESD effects on IGBTs.

Today it is not clear what impact ESD and Electrical Overstress (EOS) events have on long term reliability parameters (Vashchenko, 2008). Questions arise, such as whether there is a critical stress regime in which EOS will cause no impact; whether the EOS effect is cumulative; what changes are created in the device; what the physical mechanism of this change formation is; what drives potential accelerated degradation; and how these effects impact different devices, such as CMOS, BiCMOS and/or discrete components. Thus, what is needed is a cross-disciplinary collaboration that brings together elements from reliability engineering, understanding of EOS and nonlinear physics modeling. Progress in this direction might ultimately enable implementation of real-time algorithms for in-situ diagnostics and prognostics of power electronics systems.

The purpose of this study is the exploration of failure degradation mechanisms and damage propagation mechanisms for power semiconductor devices, where possible micro-structural defect formation due to ESD and EOS events during test and application have possible impacts on the nominal operation of these devices.

In section 2, we present background details on the functioning of IGBTs in order to aid in the understanding of our methodology for ESD damage detection and analysis. Subsequently, a physical device simulation is reported in section 3. In this simulation, the impact of local structural defects on a simplified 200V IGBT model is investigated. Here, a two-transistor model represents the power transistor with a defect. The electric characteristic curves from these simulations are then compared with experimental results to understand the underlying the physical damage caused by ESD. In Section 4, we discuss several commercially available 600V IGBTs that were tested in ESD stress experiments to demonstrate that local damage can be introduced that has parameters similar to local defects. The types of the defects are discussed in the section 5 followed by the conclusions to the study in section 6.

2. BACKGROUND

In this section, we present a discussion on two aspects of study and analysis of the effects of ESD on power transistors: (a) the physical and electrical effects of ESD and (b) the challenges of ESD testing methods.

2.1 ESD Effects on Power Transistors

In discrete power transistor components, such as power MOSFETs or IGBT's, the gate oxide is extremely susceptible to ESD events, unlike the case of integrated components (IC's) where in package ESD protection is usually provided, therefore when handling these devices during system assembly usually no ESD damage is realized.

A gate oxide stress above the critical voltage can cause structural damage to the gate oxide. This damage leads to leakage current levels beyond the specifications in the datasheet parameters. Alternatively, it could also cause a moderate change in the device structure that may result in failure during future switching operations. Thus, ESD damages are categorized as two types: (a) catastrophic and (b) latent.

Devices with catastrophic damage are those that have been instantly destroyed at the time of the ESD event and therefore will not pass the functional tests that are part of a manufacturing or repair test process. Latent damage occurs in devices when ESD degrades the device but not to the point of destroying it. In this case the changes in the power device structure are local and deviations of the characteristics due to the change in the local region are hard to detect. Therefore, these devices could generally pass the functional tests, but are expected to fail afterwards either due to further ESD events, or other forms of EOS, such as accelerated aging (Sonnenfeld et al., 2008). In addition, such devices could also suffer from a change in the safe operating area (SOA) thereby reducing the device robustness in the application regimes.

Gate oxide overstress due to ESD events can cause breakdown of the dielectric at the gate. When the device is subjected to a gate-to-source voltage high enough to arc across the gate dielectric, a microscopic hole is burnt through the gate oxide. This exposes the corresponding gate capacitor to a high electric discharge which permanently destroys the device. The smaller a device (e.g., with total width ~100-1000μm) the more susceptible it is to ESD damage. This is because a smaller device has smaller capacitance at the gate which would allow a small voltage to quickly charge the device to critical levels. Note that in many cases, immediate failure does not occur until the gate-to-source voltage exceeds the rated maximum by an amount that may be in the range of two to three times the rated maximum. This is due to the fact that the capacitance of the semiconductor device body carrying the charge tends to be much lower than the gate-source capacitance of the MOSFET, so that when the charge is transferred, the resulting voltage is much lower than the original.

During manufacturing of the device, structural defects can in general be assumed to be well controlled. Nonetheless, a small probability of a priori defects remains (Davidson, 2006; Desineni and Blanton, 2005; Khatir et al., 1994; Li and Huang, 2009; Sonnenfeld et al., 2008; Toh et al., 2008). For discrete power device arrays the detection of these defects is hard. An acceleration of the degradation processes can be expected for devices with a priori defects which manifest themselves in an increased electric field, current density and Joule heat generation. Defects that are in contrast induced during the operation of the device are hard to predict.

2.2 Challenges in ESD testing

Electronic components are required to pass some standard ESD tests on certified equipment while remaining functional. Similarly, long term reliability parameters (for example, the mean time before failure) of microelectronic components are verified by statistical methods on a limited set of components. Likewise, SOA parameters are confirmed only on a limited amount of samples.

Since most of the above testing methodologies involve subjecting the device to extreme electrical overstress events, it is advised that the components subjected to the test not be further used in the field even if they pass the tests. The intuitive reasoning for this is the possible impact of the test on long term reliability parameters. For example, if the component has been tested for pulsed SOA or zapped with an ESD tester then it incurs significant damage. In many cases, the damage would be latent. Thus, it may pass the test within the specification limits, but the latent damage may cause a failure later on.

This signifies that testing for ESD robustness is extremely difficult. This is because repeatedly subjecting the device to ESD events with intermediate parameter testing is not reliable; the tests themselves can damage the device before showing the damage caused by the ESD events. To the best of our knowledge, no technology exists that enables a repeated diagnostic of such electrical damages, since the impact of a sequence of diagnostic tests on the operational lifespan and its long term reliability is not yet well understood. Only a statistical sampling for a group of devices can currently be done using existing technologies.

Most ESD protection provided by manufacturers is primarily to protect the components during handling, packaging and assembly. Thus, even if the devices withstand ESD events initially, their long term operation and lifetime may be impacted in real-life applications involving electrical stress.

3. NUMERICAL SIMULATION

In this section we present a summary of a numerical simulation model and results for the devices under test. This model will allow for a more comprehensive understanding of the damage caused by ESD. The simulation served to test the hypothesis that ESD causes local damage during ESD discharge. Different types of physical representation for damage scenarios were simulated to different parts of the device. For simplification of the numerical analysis, an isothermal case was considered, thereby ignoring adiabatic temperature rise caused by ESD stress.

The numerical analysis was accomplished using DECIMM^{TM} (Angstrom 2009) numerical simulation framework. A two-dimensional parameterized device structure was defined using an analytical implant profiles definition. Then a set of the equations for a drift-diffusion model was solved for the most typical

parameters of the Silicon material at room temperature conditions. In addition to typical mobility models (Effect of the Strong Electric Field, Low Field Mobility), the set models included the model for recombination (Shockley-Read-Hall Generation-Recombination, Auger Recombination,) and impact ionization. The three equations of the drift diffusion model included a Poisson's equation and two continuity equations for electrons and holes.

In most electronic circuits, heat dissipation mechanisms are provided which mitigate the effects of such temperature rise. Thus, the effects of heating from ESD events can be considered to be of less significance compared to deviations in electric characteristics due to physical changes in the semiconductor die.

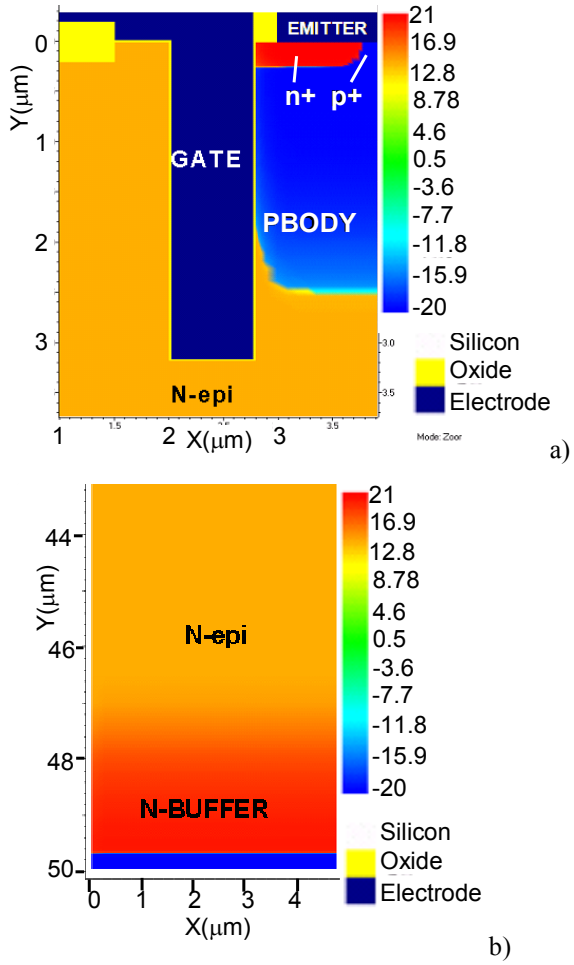


Figure 1. Simplified simulation cross-section for the (a) upper and (b) lower part of the IGBT device used for numerical analysis of the experiment test data.

The device cross-section is shown in Figure.1. The two-dimensional device cross-section model (Figure.1) displays the typical architecture for a vertical gate (trench gate) IGBT cell. The upper region (Fig.1a) of the device has shallow source and body n+ and p+ diffusion regions along with the second p-body diffusion that forms the well of the vertical N-channel MOS device. The poly-silicon gate is separated by the thin gate oxide (yellow border outlining the blue gate region) from the silicon. The right part of the cross-section (Figure.1a) represents the active device while the left part represents the lateral termination of the array. Figure 1b shows the lower part of the device that forms the emitter. This typical MOS structure provides an accumulation channel when there is positive gate bias applied above the device threshold voltage level.

Figure 2 shows the switching characteristics of the device as obtained from the simulation of the model shown in (Figure 1).These switching characteristics show the standard switching behavior of a normal device.

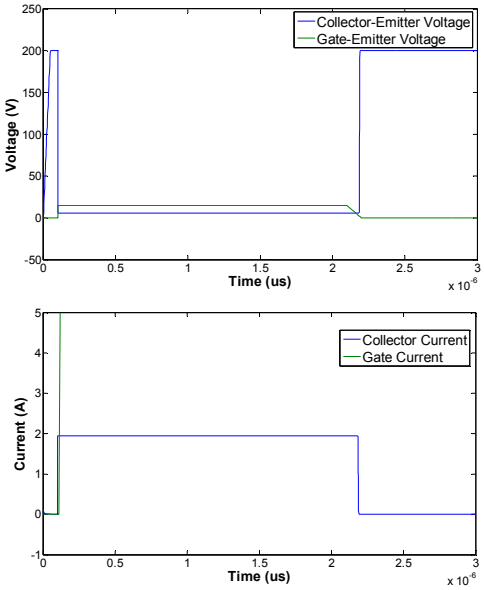


Figure 2. Switching characteristics of the standard devices.

In Figure 3, the output characteristics of the device at 5V collector voltage is shown with threshold voltage ~0.9V and saturation current $i_C \sim 5e^{-5}$A. The total current level for the device is normalized for $w = 1\mu m$ structure width:

$$I = Sxi_C / (lw)$$
$$= (10^6 \mu m^2)x(5x10^5 A)/(5\mu m x 1\mu m) = 10A, \quad (1)$$

where S, i_C, w, l are the total die active area, simulated saturation current of the segment, simulated segment cross-section length, and 1 μm width, respectively. The trans-conductance characteristics of the device for different P_{BODY} lengths are shown in Figure 4.

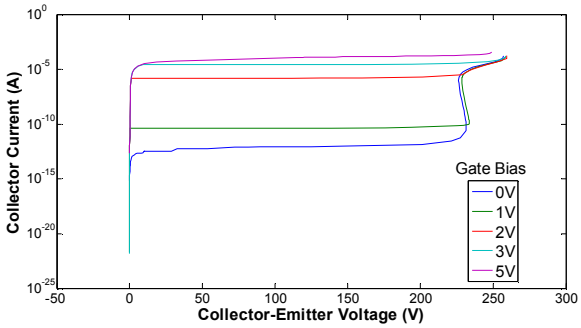


Figure 3. Output IC-VCE characteristics of initial device.

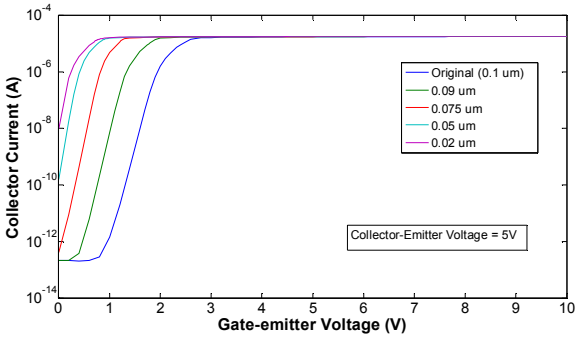


Figure 4. IC-VGE at different PBODY profile lengths.

The approximate model for a transistor with defects is shown in figure 5 which we refer to as the mixed mode representation. The mixed mode simulation case for a defective device can be represented by the cross-section with a width scaling factor w_i = 2x10^{5}µm and the additional cross-section with the parameter deviation for defective device w_d varying from 1 to 1µm.

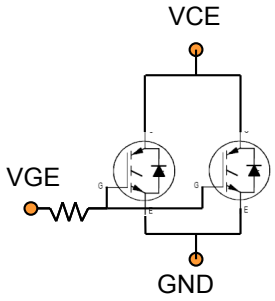


Figure 5. Mixed mode representation for the device with a local defect.

Figure 6 shows the output characteristics of a device with doping deviation in the N-epi layer, while the trans-conductance variation in the device due to doping deviation is shown in figure 7.

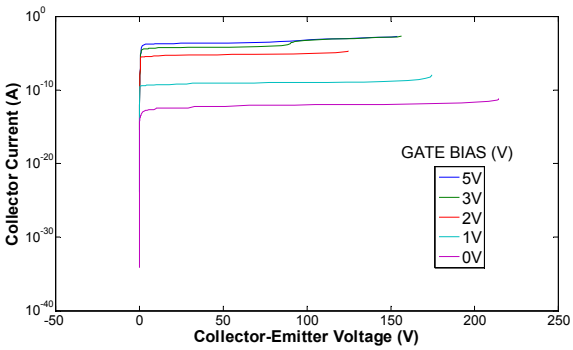


Figure 6. Output IC-VCE characteristics of the devices in case of the N-epi doping deviation.

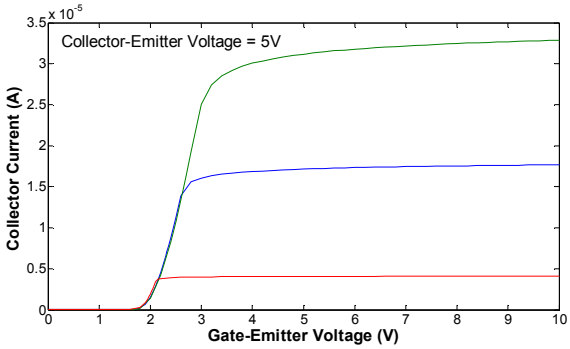


Figure 7. Output trans-conductance IC-VGE for different N-epi doping deviation.

A comparison of the output characteristics of the normal device (figure 3) with the devices with N-epi doping deviation (figure 6) shows significant change in the characteristics. Similarly for the trans-conductance curves for the normal device vary considerably compared to the defective device where the devices turn on at a higher gate-emitter voltage.

The effects of local faults i.e., localized N-epi doping deviations were also simulated and are shown in figures 8 and 9 which present the output characteristics and resulting trans-conductance respectively. Clearly, such local defects introduce slight changes in the characteristic curves, such as the slight increase in collector current at approximately 230V compared to normal device as shown in figure 8. Similarly, a small change due to local doping deviation occurs in the trans-conductance curve at gate-emitter voltage of approximately 2V when compared with the normal device. These device electrical characteristics (figures 8, 9) will be used for comparison with electrical characteristics of ESD damaged devices from experiments. Since it is suspected that ESD events create local damage sites, the characteristics of a damaged device are expected to show electrical characteristics similar to that simulated for a device with local damages as shown in figures 8 and 9.

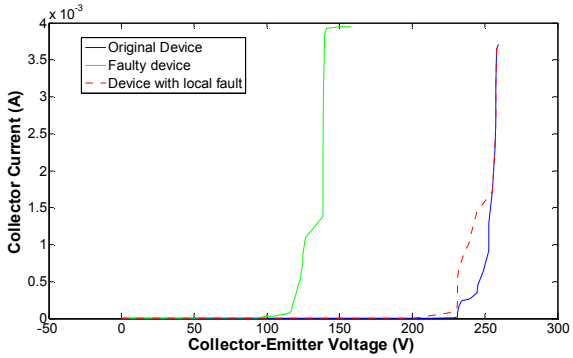


Figure 8. Output characteristics of faulty device with localized doping deviation.

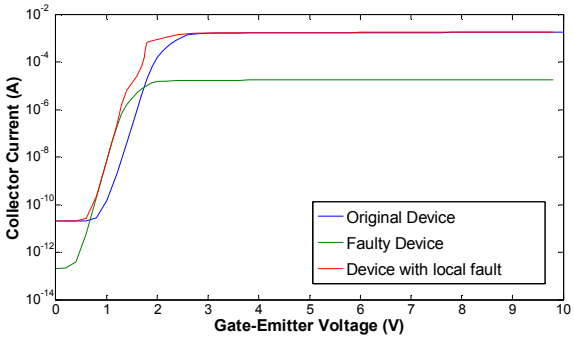


Figure 9. Trans-conductance of faulty device with localized doping deviation.

4. EXPERIMENTAL STUDY OF THE PULSED EOS EFFECT

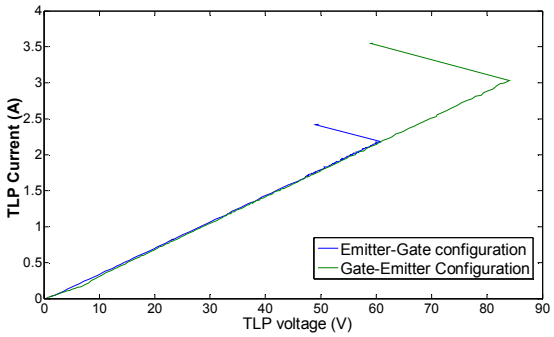
The device chosen for experimental stress testing is the IRG4BC30KD. This device has typical structure of a vertical gate (trench gate) IGBT cell (Figure.10) with a package integrated fly back diode. The figure clearly shows two separate dies, one of which contains the IGBT while the other forms the protective diode.

Figure 10. IRG4BC30KD de-capped view of the IGBT die.

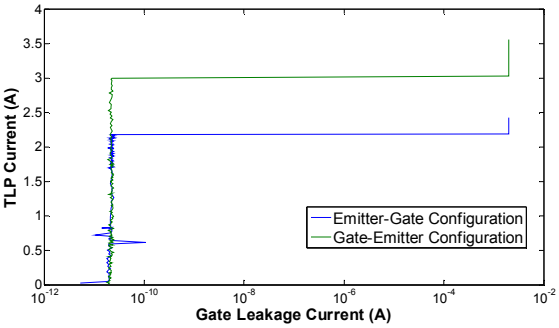
4.1 TLP stress experiments

In this section, we summarize our ESD damage detection and testing mechanism using Transmission Line Pulse (TLP). The goal of conducting TLP measurements is to explore whether limited stress introduces local defect(s) within the device. Note that TLP measurements up to failure can be considered as a form of an EOS event. In the case of the collector-emitter TLP characteristics, the devices under experiment were measured with the TLP coaxial line connected directly to the collector terminal and the TLP ground to the emitter terminal. The gate terminal was connected to an external power supply. The maximum pulsed voltage amplitude of the TLP system is 500 V and provides approximately 10Amps at 50 Ohm load.

The hypothesis was that during TLP testing, the gate oxide would be overstressed creating gradual changes in the device structure. This would result in changes in the device characteristics that are beyond normal values but lie within the device datasheet parameters maximum limits such that these devices can be subjected to further accelerated aging test experiments. Such tests would aid in exploring changes in its aging behavior. However, it was observed that the above is not always true as shown in figure.11. In the figure, it may be observed that for two of the experimental samples, the above expectation did not hold as they demonstrated significant gate leakage current as well as deviation in their TLP voltage-current profiles. The damage of the power array during critical stress conditions has catastrophic nature both for positive and negative TLP gate overstress.



(a)



(b)

Figure 11(a, b). Positive pulsed (TLP) gate-emitter characteristics of the IGBT devices subjected to gate ESD overstress.

In the test case of gate-emitter TLP operation, it was observed that the device holds approximately three times the amount of voltage specified by the maximum limit rating. It may be noted that such voltage levels can easily be achieved during handling of the device at

system assembly. Gradual damage which might be seen as a detectable change in the leakage current (measured between TLP pulses) was not observed. Note that in many instances large power device arrays fail in a catastrophic manner due to formation of big internal parasitic capacitor charge that provides significant current through the formed local defect.

4.2 ISO system level pulses

In this section, our methodology for introducing ESD damage using an International Organization for Standardization (ISO) gun device is described. The ISO gun was used in order to overcome TLP system limitations during the collector-emitter ESD stress test of the IGBT device. There are two major modes for the operation of the gun – direct electrical contact discharge and air gap discharge. An initial pre-test was carried out in order to determine the ESD levels required to produce detectable damage for different configurations.

For the initial pool of samples, the leakage level observed after ESD zapping was consistently lower than the maximum limit of the datasheet parameters by several orders (0.01uA vs. 250uA). The breakdown voltage had variation around two different levels, 650V and 665V at room temperature, which is above the datasheet maximum rating limit of 600V. No failures were observed below a certain ESD pulse threshold level even when up to 100 pulses were applied.

ESD pulse was applied to the collector - emitter junctions. The reverse current paths in IGBTs are protected by the package level integrated diode and hence they can withstand a high level of electrical voltage. Prior studies show that the diode can withstand stress up to the 30kV limit of the ISO gun. Most of the exhibited collector-emitter leakage is at the level of hundreds of micro-amps to several milliamps while most of the devices still had breakdown voltage above 600V; several devices also showed reduction in the breakdown voltage. Although the device exceeded the datasheet leakage current (~250 uA) limit by a factor of 3, the sample remained fully functional with no additional gate leakage current. Primarily, two typical modes of fault generation were observed for ESD pulses above a certain threshold level. These involved localized defect formation causing deviation in device parameters but no catastrophic failures. These defect modes are described in the details in section 4.4.

The gate-emitter (G-E) ESD pulse combination damaged the device irreversibly and catastrophically in case of contact zap. Experimental data for the gate collector combination – (G-C) air gap zap – were collected for the samples and stored for future accelerated tests to measure time to failure parameters.

The output characteristics for the tests with different configurations as well different modes of failures are presented in the following sections. We first present our results from applying ESD stress at the collector-emitter junctions in section 4.3 followed by the results from the stress applied to the gate-collector junctions in section 4.4.

4.3 Collector-Emitter (C-E) Zap Electrical Test data

The electrical data comparison before and after C-E zap are presented in figures 12 (a-d). As expected, majority of the samples have the leakage-breakdown characteristics that correspond to formation of a localized region with a current level ~1 mA. This localized defect can form in the vertical emitter collector junction either between the P_{BODY}–N-epi regions or it could correspond to damage of the n-buffer region.

Two typical modes for non-catastrophic parametric failures were observed for pulses above a certain ESD threshold level. For the first mode, the characteristics shown in Figures 12a, b exhibit similarities with the output characteristics obtained from the simulation of the mixed-mode models involving local damages, such as buffer deviation or N-epi doping deviation as shown in figures 8 and 9. The sudden increase in collector current at approximately 320V in figure 12a is similar to the change shown in figure 8 earlier while the change in transconductance characteristics observed in Figure 12b is similar to the characteristics shown in Figure 9. These variations mainly represent the case when both the MOS and the buffer structure have been affected.

In contrast, for the second mode of damage, samples shown in figures 12 (c, d) have a change only in the leakage state which could be due to damage in the termination region. Additional measurements are required to determine the nature of the changes.

4.4 Gate-Collector (G-C) Tests

For gate-collector stress, the comparison of ET data before and after ESD stress leads to the conclusion that the failure signature is completely different compared to C-E stress. The ET data have been collected at ~1 mA peak current limitation, based upon curve trace data. The output characteristics are shown in figure 13 (a-b).

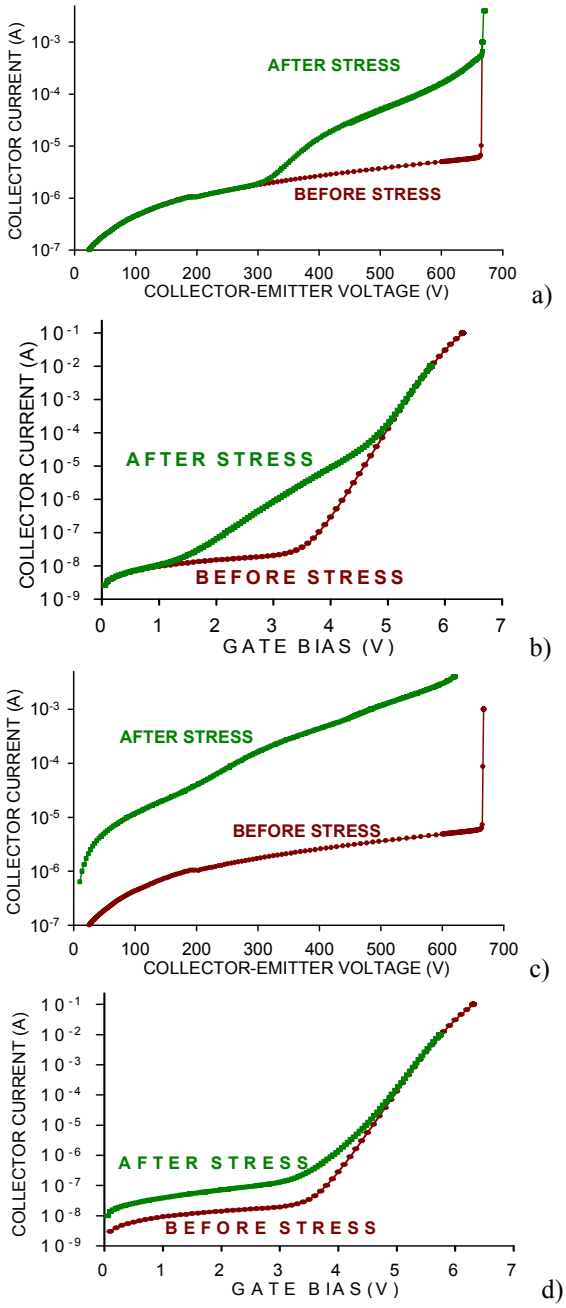


Figure 12. (a) Comparison of collector-emitter output characteristics for first mode of non catastrophic failure, (b) Corresponding transconductance characteristics (c) Comparison of collector-emitter output characteristics for second mode of non catastrophic failure, (d) Corresponding transconductance. The comparisons are between characteristics obtained before and after ESD stress for the two typical IGBT samples.

From these figures, it can be observed that most of the samples have elevated leakage current, while the breakdown voltage remains unchanged. This indicates that the MOS structure has incurred damage, rather than the collector junction.

The level of change in the collector current as well as trans-conductance indicates more severe damage as compared to the results obtained from the ESD zaps applied to the CE junction. Additional electrical test data are required to determine whether the leakage is generated in the gate current path or located purely in the MOS structure bulk-emitter region.

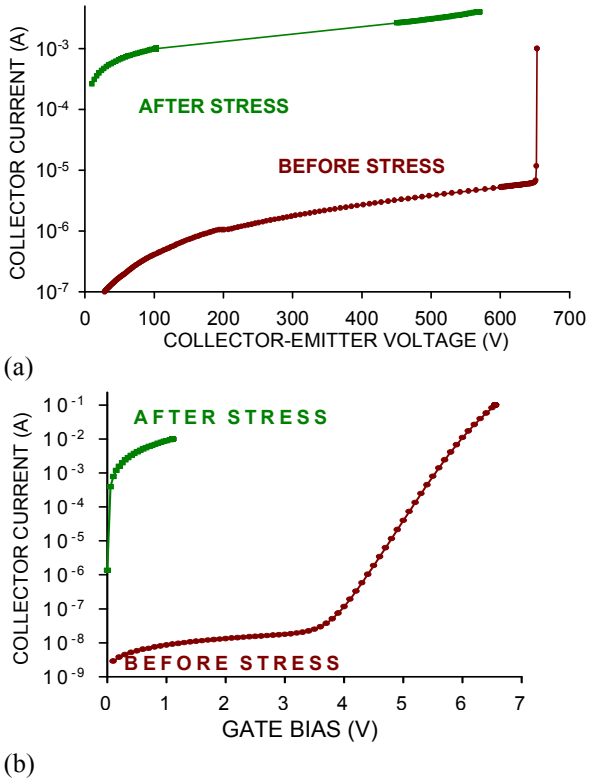


Figure 13. Change of the (a) output characteristics and (b) transconductance as a result of gate-collector air gap stress.

5. CONCLUSION

It was demonstrated how at certain ESD magnitude levels, damage of discrete power devices were observed prior to catastrophic failure. While these damages manifest themselves as changes to SOA, they cannot be detected as significant deviation of device parameters beyond the datasheet electrical parameter limits.

Contact zaps applied to the gate-emitter (G-E) combination can cause irreversible damage of the device with ESD settings as low as 1kV. In contrast, the collector-emitter (C-E) and gate-collector (G-C) ESD stress combination is able to withstand damage at that level without inducing junction damage until considerably higher ESD settings are used.

It was hypothesized that the ESD causes local damage. To test the hypothesis, two types of local damages were simulated related to the local doping deviation in the collector N-epi and buffer region and the CMOS structure regions. The changes of the tests observed in the output and the transconductance characteristics correspond (for a subset of all experiments) to the simulated localized damages.

The results obtained and the test methodology proposed in this study will be useful for damage modelling in a prognostic context. The results may also aid in robust design of electronic components.

Future work includes exploration of accelerated tests that will allow the identification of changes in ET parameters that can be used as precursors for imminent irreversible failures. Those features will be used to estimate remaining useful life times of the devices in a system health management setting.

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